

Compal Confidential

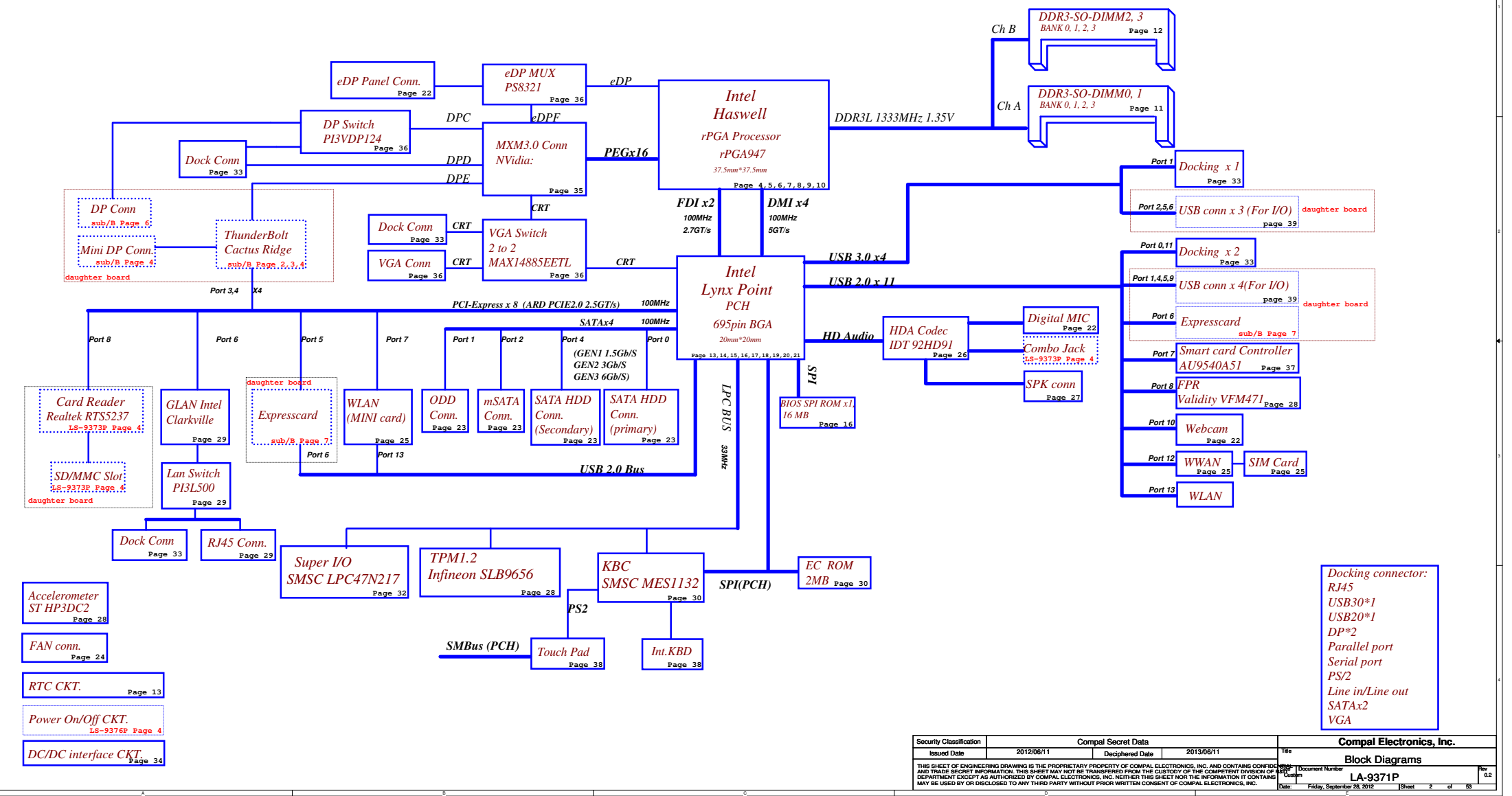
Intel Haswell rPGA Processor with Lynx Point-H Afterburn MXM LA-9371P

2012-09-28

REV : 0.2

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/06/11	Deciphered Date	2013/06/11	Title	Cover Page
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				Date Friday, September 28, 2012	Sheet 1 of 53

Model Name : Afterburn
File Name : LA-9371P



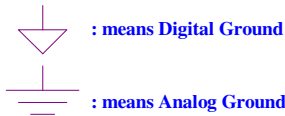
Docking connector:
RJ45
USB30*1
USB20*1
DP*2
Parallel port
Serial port
PS/2
Line in/Line out
SATAx2
VGA

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Voltage Rails (O MEANS ON X MEANS OFF)

<div>power plane</div> <div>State</div>	+RTCVCC	B+	+5VDS +3VDS	+1.35V +0.675VS	+5VS +3VS +1.5VS +VCC_CORE +1.05VS +1.05VM	
S0	O	O	O	O	O	
S1	O	O	O	O	O	
S3	O	O	O	O	X	
S5 S4/AC	O	O	O	X	X	
S5 S4/ Battery only	O	O	X	X	X	
S5 S4/AC & Battery don't exist	O	X	X	X	X	

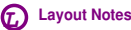
Symbol Note :



@ : means just reserve , no build

AMT@ : means just install for support iAMT

CONN@ : means ME part.



Layout Notes

07/24 update



: Question Area Mark.(Wait check)

Install below 45 level BOM structure for ver. 0.1

45@ : means just put it in the BOM of 45 level.

Install below 43 level BOM structure for ver. 0.1

DEBUG@ : means just build when PCIE port 80 CARD function enable.Remove before MP

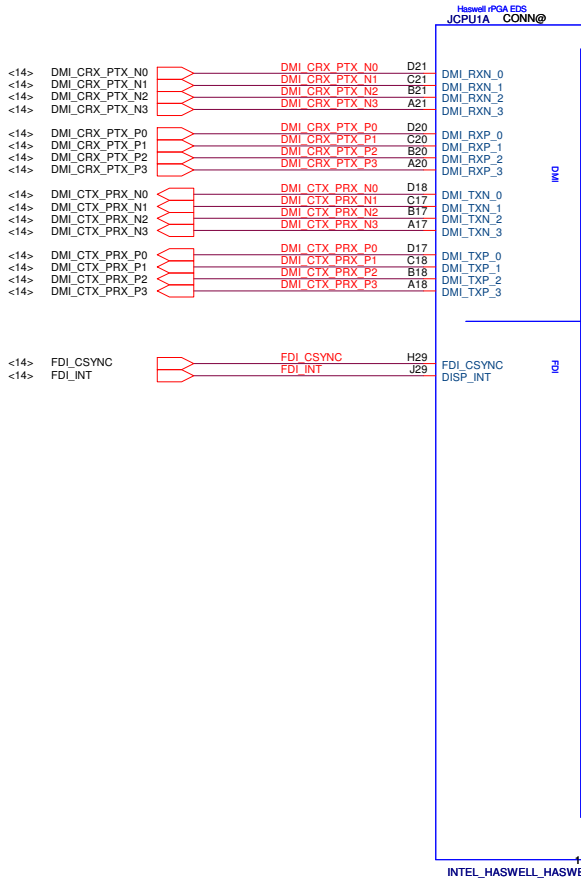
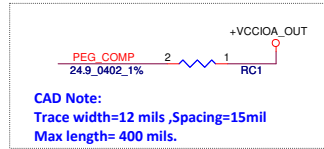
SMBUS Control Table

	SOURCE	BATT	2nd BATT	XDP	SODIMM	G-SENSOR	TP	NIC	NFC	EC	MXM
I2C_MAIN_CLK I2C_MAIN_DAT	SMSC1126	V	X	X	X	X	X	X	X	X	X
I2C_BAY_CLK I2C_BAY_DAT	SMSC1126	X	V	X	X	X	X	X	X	X	X
MEM_SMBCLK MEM_SMBDATA	Haswell	X	X	V	V	V	V	X	X	X	X
LAN_SMBCLK LAN_SMBDATA	Haswell	X	X	X	X	X	X	V	V	X	X
SML1_SMBCLK SML1_SMBDATA	Haswell	X	X	X	X	X	X	X	X	V	V

Stapping Options Flash

GPIO 51 Bit 1	GPIO 19 Bit 0	Boot BIOS Destination
0	0	Reserved
0	1	RSVD
1	0	SPI
1	1	LPC

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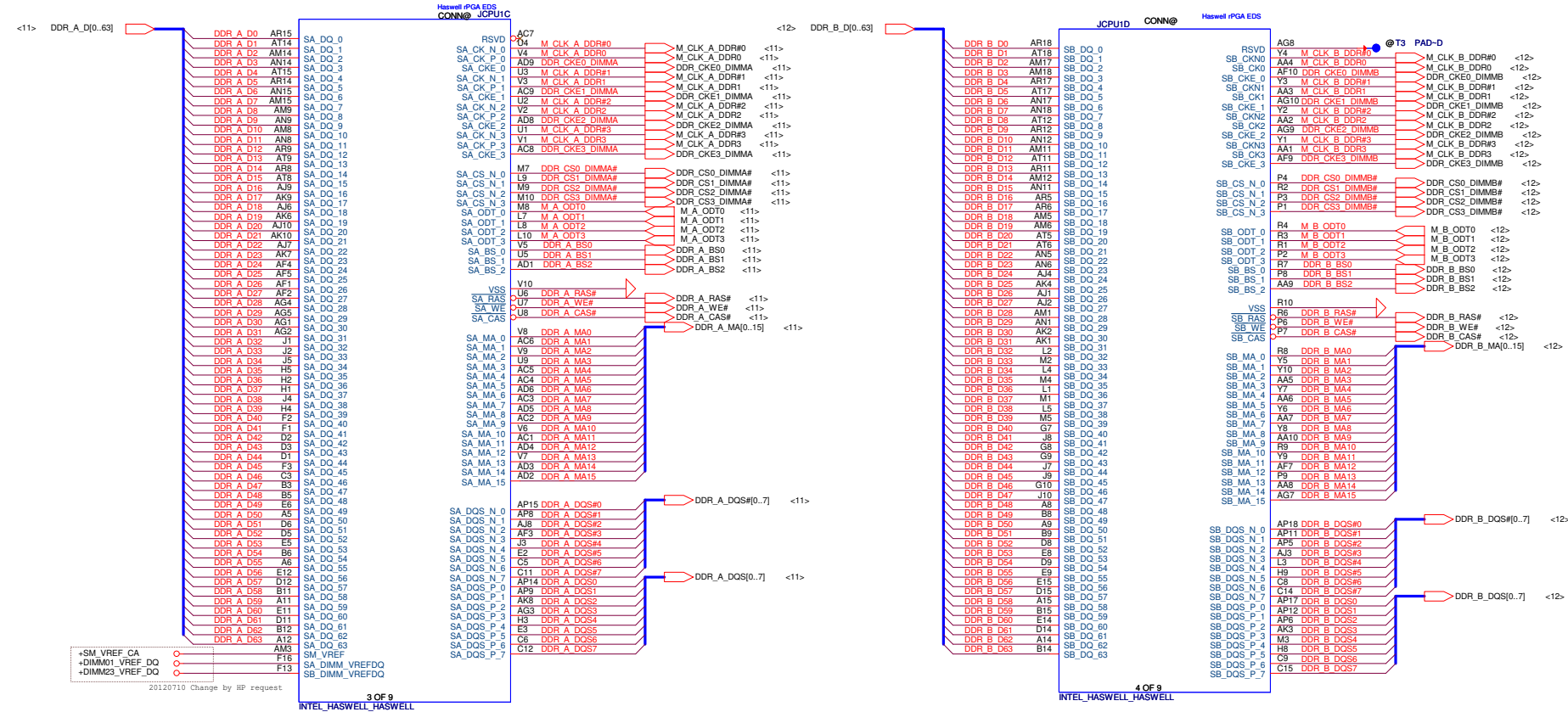


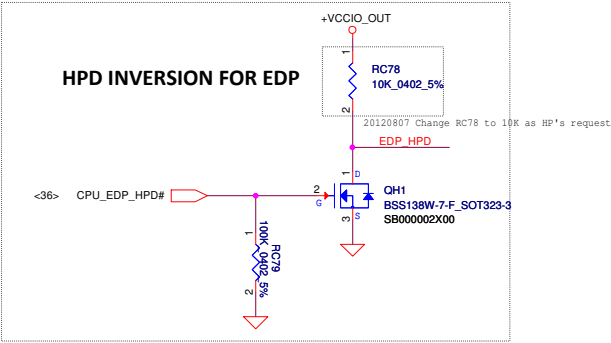
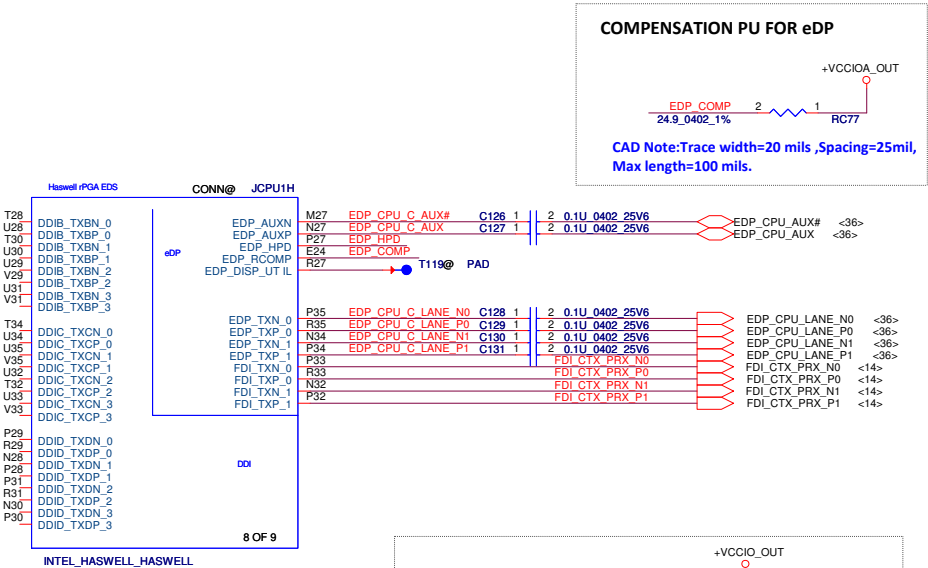
PEG_CRX_GTX_P[0..15]	PEG_CRX_GTX_P[0..15]	<35>
PEG_CRX_GTX_N[0..15]	PEG_CRX_GTX_N[0..15]	<35>
PEG_CTX_GRX_P[0..15]	PEG_CTX_GRX_P[0..15]	<35>
PEG_CTX_GRX_N[0..15]	PEG_CTX_GRX_N[0..15]	<35>

PEG_CTX_GRX_C_P0	CC1	2	1	0.22U	0402	6.3V6K	PEG_CTX_GRX_P0
PEG_CTX_GRX_C_N0	CC2	2	1	0.22U	0402	6.3V6K	PEG_CTX_GRX_N0
PEG_CTX_GRX_C_P1	CC3	2	1	0.22U	0402	6.3V6K	PEG_CTX_GRX_P1
PEG_CTX_GRX_C_N1	CC4	2	1	0.22U	0402	6.3V6K	PEG_CTX_GRX_N1
PEG_CTX_GRX_C_P2	CC5	2	1	0.22U	0402	6.3V6K	PEG_CTX_GRX_P2
PEG_CTX_GRX_C_N2	CC6	2	1	0.22U	0402	6.3V6K	PEG_CTX_GRX_N2
PEG_CTX_GRX_C_P3	CC7	2	1	0.22U	0402	6.3V6K	PEG_CTX_GRX_P3
PEG_CTX_GRX_C_N3	CC8	2	1	0.22U	0402	6.3V6K	PEG_CTX_GRX_N3
PEG_CTX_GRX_C_P4	CC9	2	1	0.22U	0402	6.3V6K	PEG_CTX_GRX_P4
PEG_CTX_GRX_C_N4	CC10	2	1	0.22U	0402	6.3V6K	PEG_CTX_GRX_N4
PEG_CTX_GRX_C_P5	CC11	2	1	0.22U	0402	6.3V6K	PEG_CTX_GRX_P5
PEG_CTX_GRX_C_N5	CC12	2	1	0.22U	0402	6.3V6K	PEG_CTX_GRX_N5
PEG_CTX_GRX_C_P6	CC13	2	1	0.22U	0402	6.3V6K	PEG_CTX_GRX_P6
PEG_CTX_GRX_C_N6	CC14	2	1	0.22U	0402	6.3V6K	PEG_CTX_GRX_N6
PEG_CTX_GRX_C_P7	CC15	2	1	0.22U	0402	6.3V6K	PEG_CTX_GRX_P7
PEG_CTX_GRX_C_N7	CC16	2	1	0.22U	0402	6.3V6K	PEG_CTX_GRX_N7
PEG_CTX_GRX_C_P8	CC17	1	2	0.22U	0402	6.3V6K	PEG_CTX_GRX_P8
PEG_CTX_GRX_C_N8	CC18	1	2	0.22U	0402	6.3V6K	PEG_CTX_GRX_N8
PEG_CTX_GRX_C_P9	CC19	1	2	0.22U	0402	6.3V6K	PEG_CTX_GRX_P9
PEG_CTX_GRX_C_N9	CC20	1	2	0.22U	0402	6.3V6K	PEG_CTX_GRX_N9
PEG_CTX_GRX_C_P10	CC21	1	2	0.22U	0402	6.3V6K	PEG_CTX_GRX_P10
PEG_CTX_GRX_C_N10	CC22	1	2	0.22U	0402	6.3V6K	PEG_CTX_GRX_N10
PEG_CTX_GRX_C_P11	CC23	1	2	0.22U	0402	6.3V6K	PEG_CTX_GRX_P11
PEG_CTX_GRX_C_N11	CC24	1	2	0.22U	0402	6.3V6K	PEG_CTX_GRX_N11
PEG_CTX_GRX_C_P12	CC25	1	2	0.22U	0402	6.3V6K	PEG_CTX_GRX_P12
PEG_CTX_GRX_C_N12	CC26	1	2	0.22U	0402	6.3V6K	PEG_CTX_GRX_N12
PEG_CTX_GRX_C_P13	CC27	1	2	0.22U	0402	6.3V6K	PEG_CTX_GRX_P13
PEG_CTX_GRX_C_N13	CC28	1	2	0.22U	0402	6.3V6K	PEG_CTX_GRX_N13
PEG_CTX_GRX_C_P14	CC29	1	2	0.22U	0402	6.3V6K	PEG_CTX_GRX_P14
PEG_CTX_GRX_C_N14	CC30	1	2	0.22U	0402	6.3V6K	PEG_CTX_GRX_N14
PEG_CTX_GRX_C_P15	CC31	1	2	0.22U	0402	6.3V6K	PEG_CTX_GRX_P15
PEG_CTX_GRX_C_N15	CC32	1	2	0.22U	0402	6.3V6K	PEG_CTX_GRX_N15

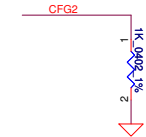
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Issued Date	2012/06/11	Deciphered Date	2013/06/11	Title	DMI, PEG	
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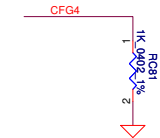




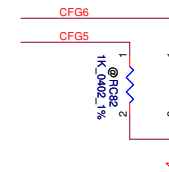
CFG STRAPS for CPU



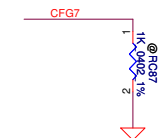
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



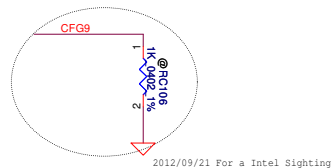
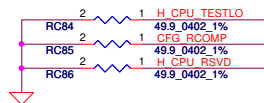
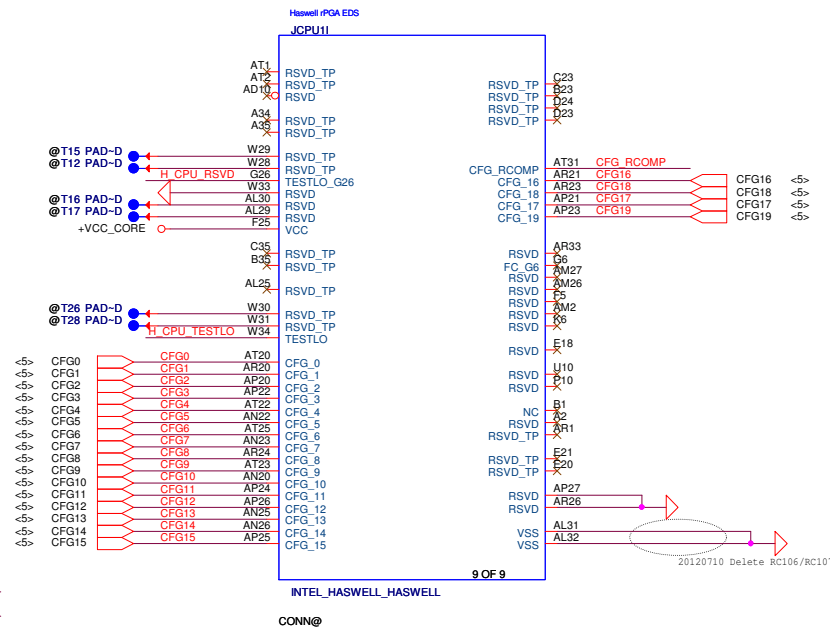
Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>

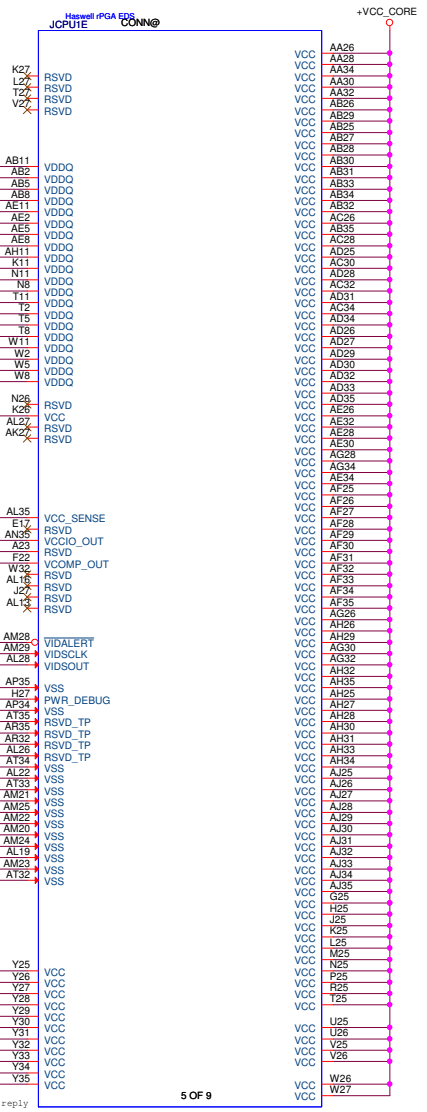
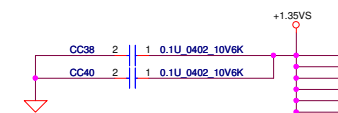


PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

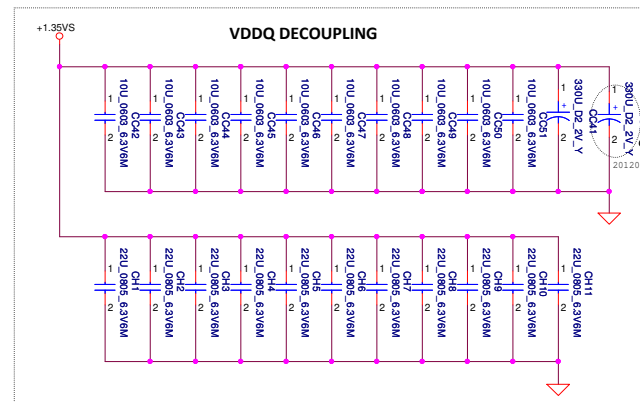
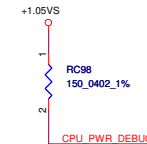


PEG DEFER TRAINING	
CFG7	<p>1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>



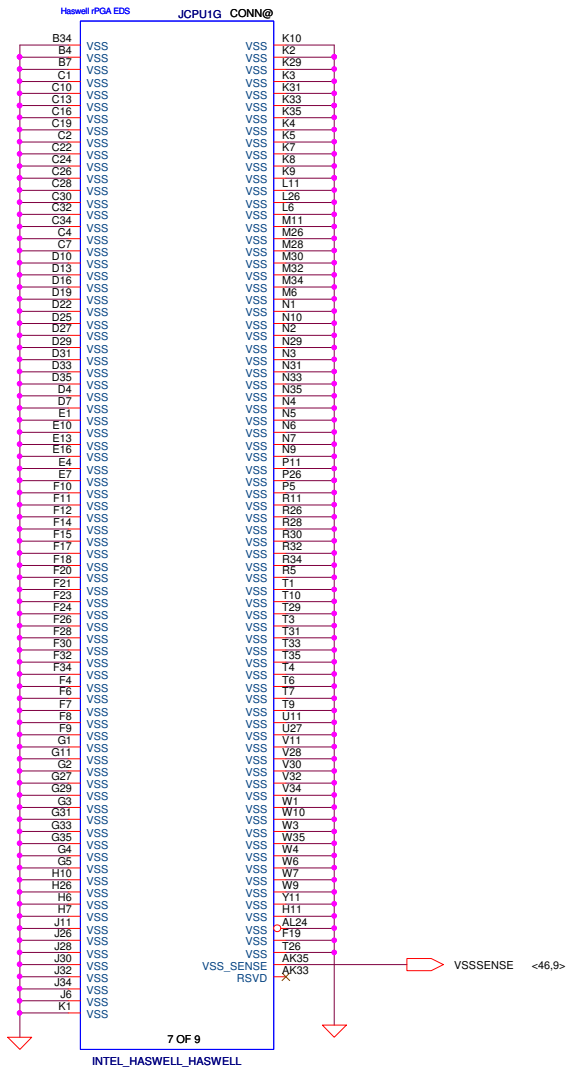
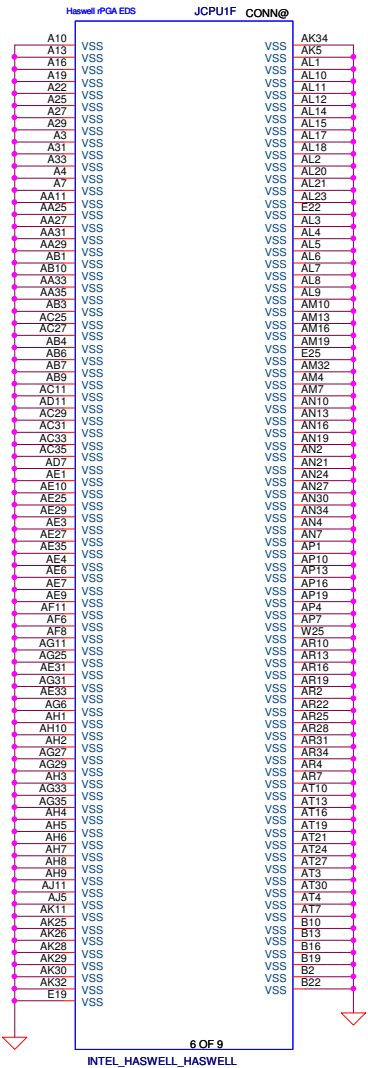


**CAD Note: Place the PU resistors close to CPU
RC63 close to CPU 300 - 1500mils**

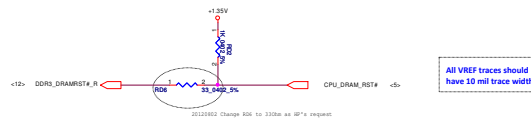


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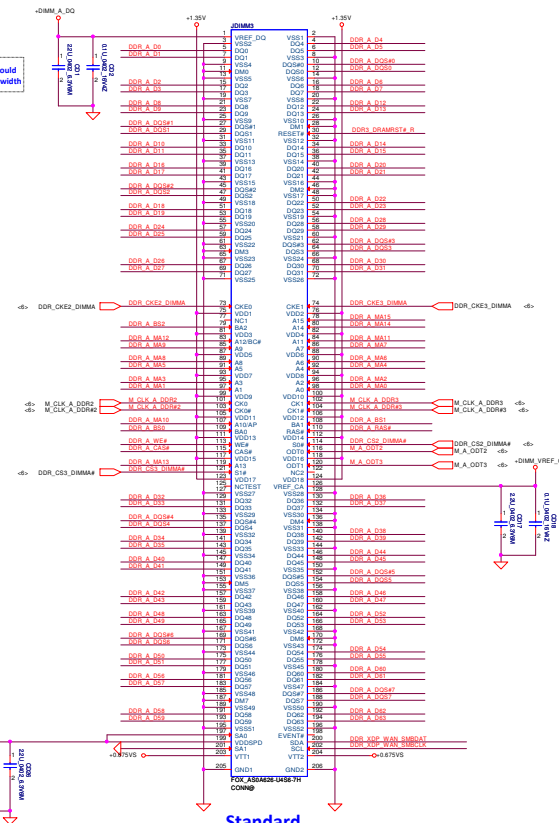
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JDIMM3 H=4.0mm BOT



All VREF traces should have 10 mil trace width



Standard

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			Printed: 2016/06/06 11:00:00	

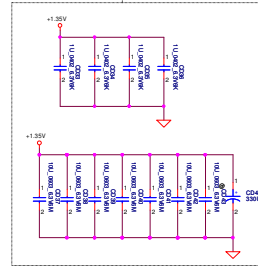
Populate R0A, De-Populate R0B for Intel DDR3 VREFDQ multiple methods M1
Populate R0B, De-Populate R0A for Intel DDR3 VREFDQ multiple methods M3

JDIMM2 H=9.2mm TOP

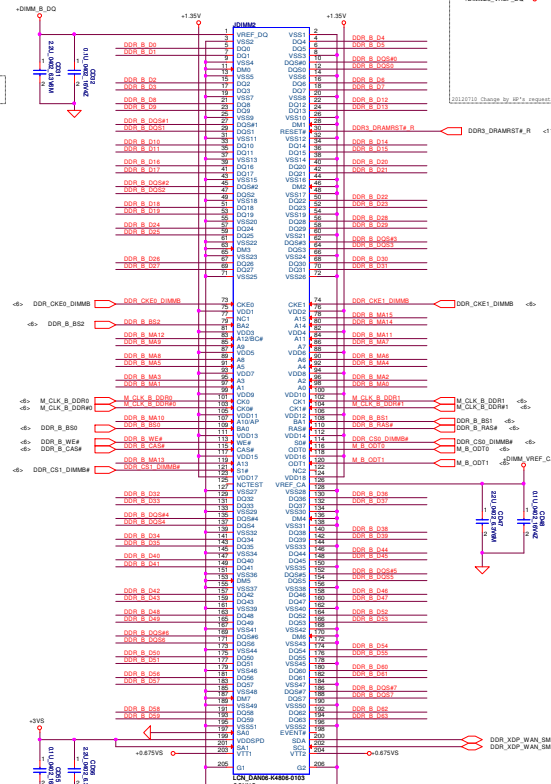
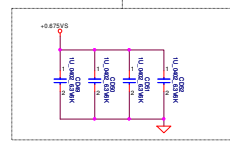
JDIMM4 H=4.0mm BOT

DDR_B_DQ[43]
DDR_B_DQS[9..7]
DDR_B_DQS[9..7]
DDR_B_M[15]

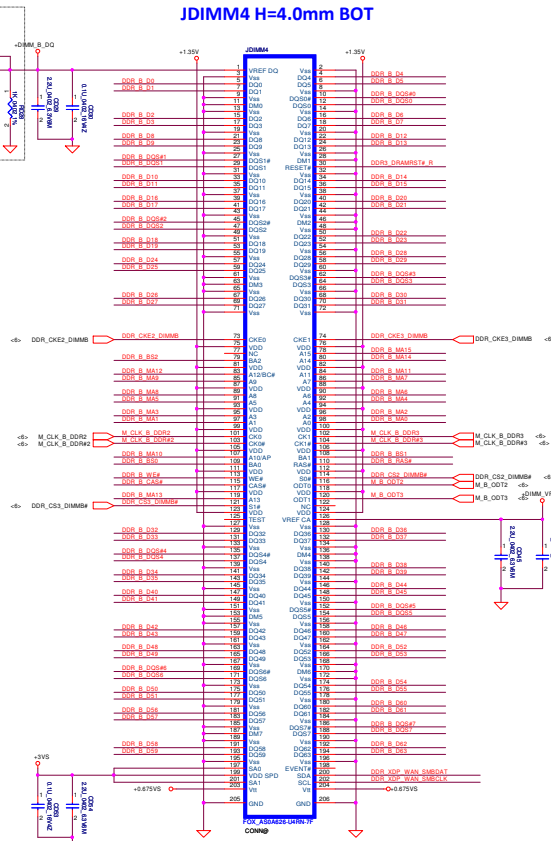
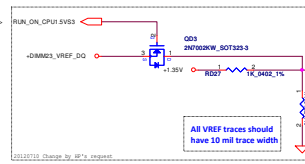
Layout Note:
Place near JDIMM2



Layout Note:
Place near JDIMM2,203,204



Reverse



Reverse

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INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
 High - Enable Internal VRs
 Low - Enable External VRs

NO REBOOT STRAP
 DISABLED WHEN LOW (DEFAULT)
 ENABLED WHEN HIGH

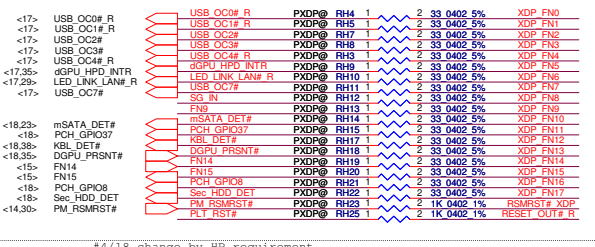
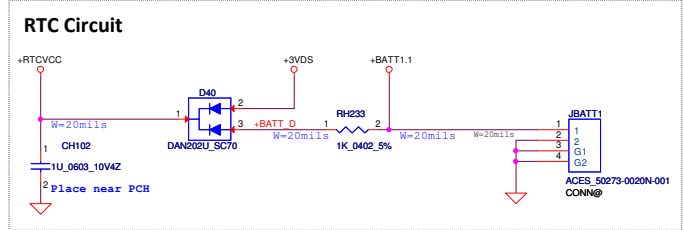
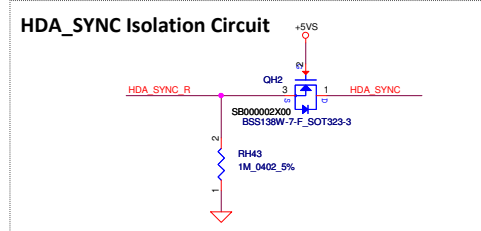
HDD HALTED
 100K_0402_5%

20120802 HP's request

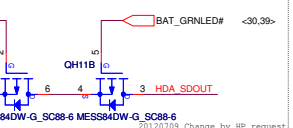
FLASH DESCRIPTOR SECURITY OVERRIDE
 LOW = DESABLED (DEFAULT)
 HIGH = ENABLED

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers



#4/18 change by HP requirement



20120709 Change by HP request

20120919 Change QH11 to PMS

20120703

20120921 HP's request

20120703

20120703

20120703

20120703

20120703

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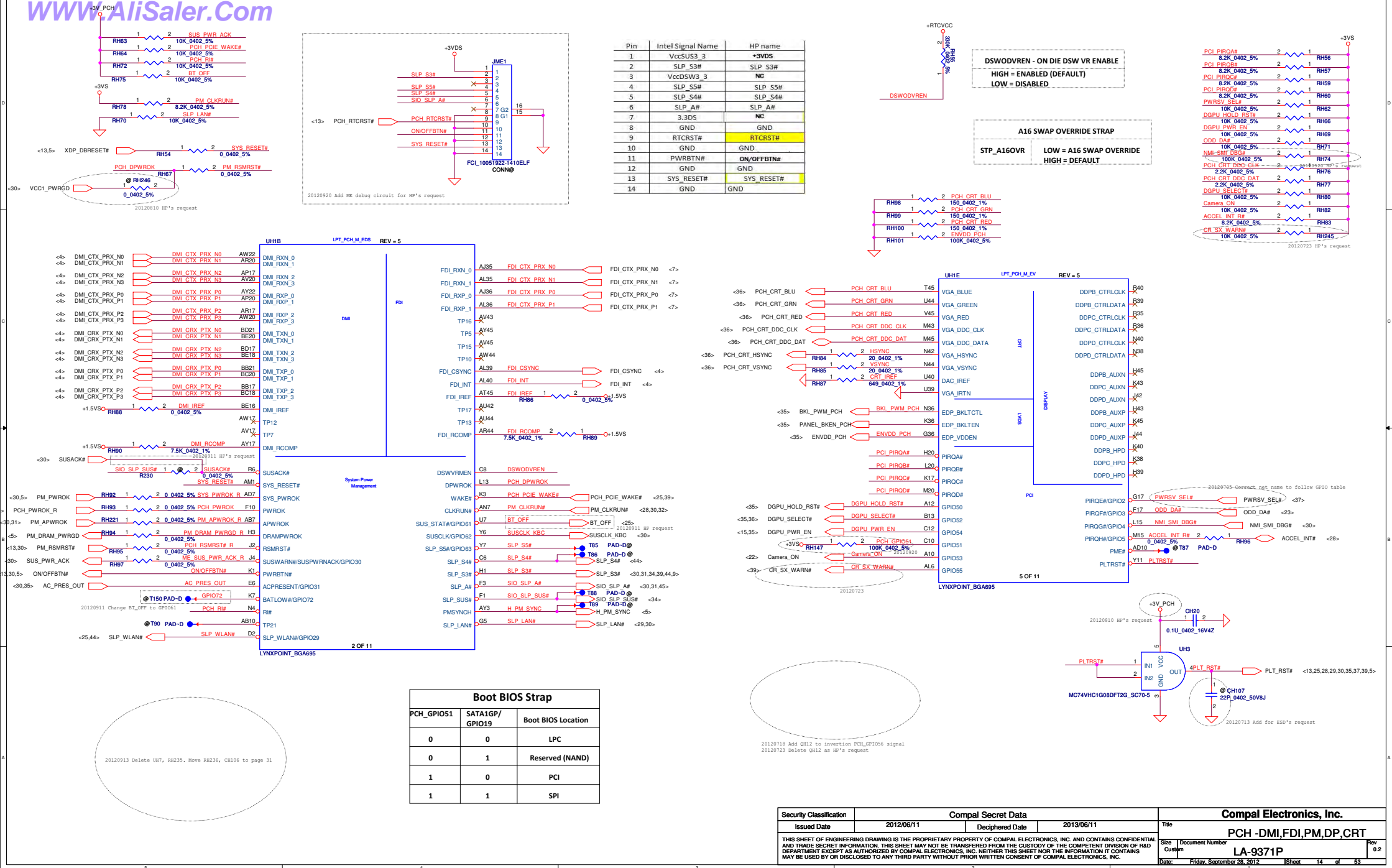
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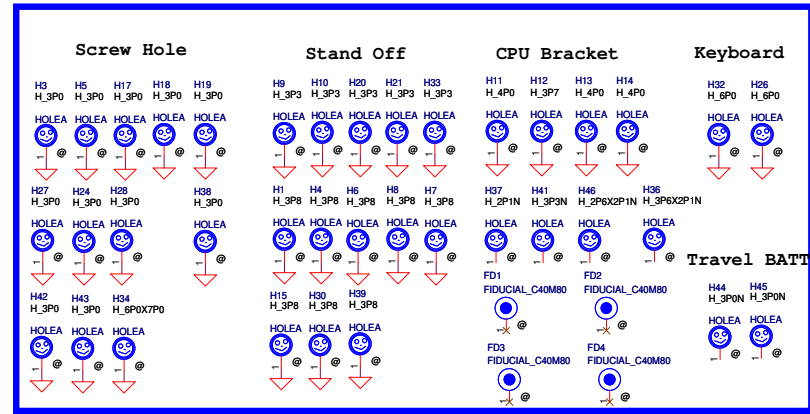
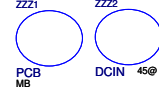
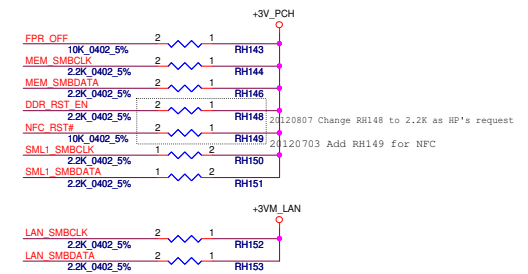
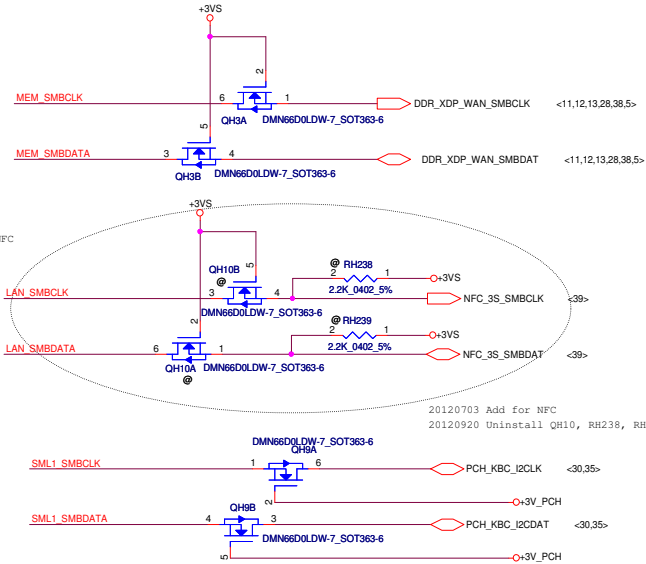
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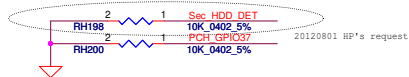
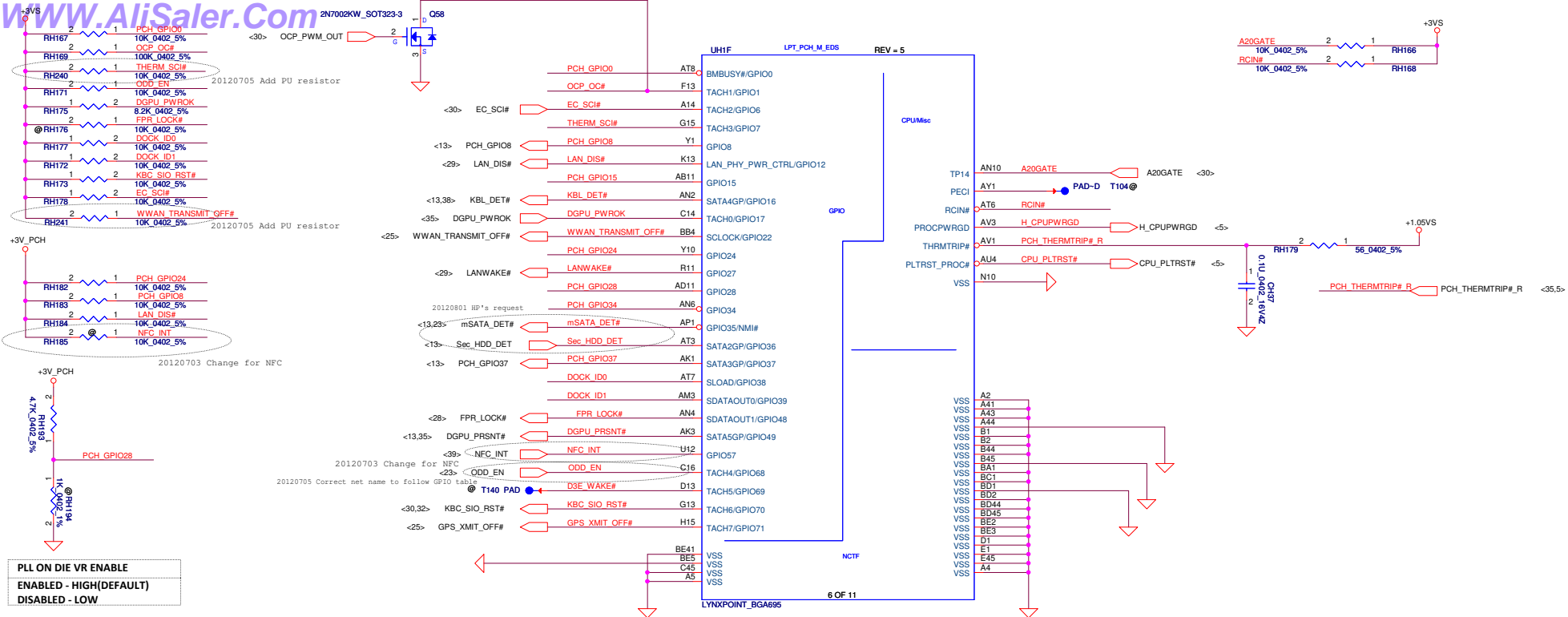


Boot BIOS Strap		
PCH_GPIO51	SATA1GP/ GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/06/11	Deciphered Date	2013/06/11	Title	PCH -DMI,FDI,PM,DP,CRT
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				Document Number	0.2
				LA-9371P	
Date:	Friday, September 28, 2012	Sheet	14	of	53

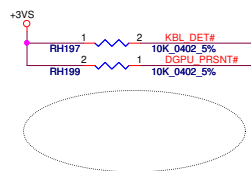


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Issued Date	2012/06/11	Deciphered Date	2013/06/11	Title		
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				Size	Document Number	Rev
				Custom	LA-9371P	0.2
Date:				Friday, September 28, 2012	Sheet	16 of 53



SATA2GP/GPIO36, SATA3GP/GPIO37 SAMPLED AT RISING EDGE OF PWROK.
WEAK INTERNAL PULL-DOWN.(WEAK INTERNAL PULL-DOWN IS DISABLED AFTER
PLRST_N DE-ASSERTS).
NOTE: THIS SIGNAL SHOLD NOT BE PULLED HIGH WHEN STRAP IS SAMPLED.

Config	GPIO16,49
USB X4,PCIEX8,SATAx6	11
USB X6,PCIEX8,SATAx4	01

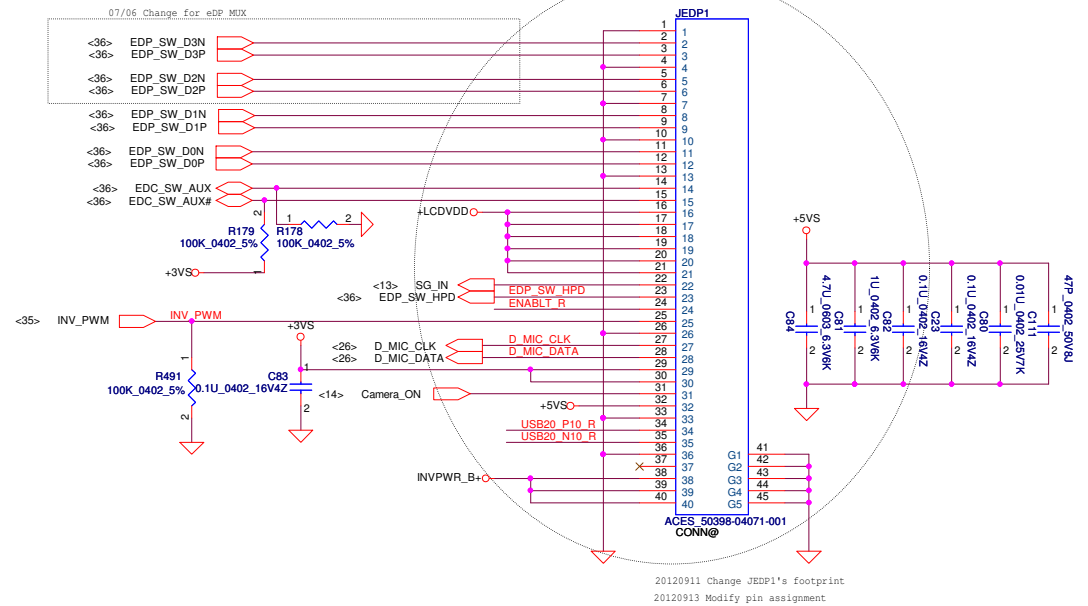
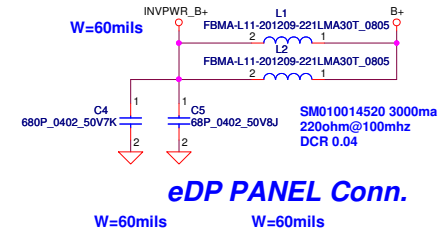
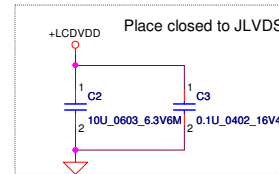
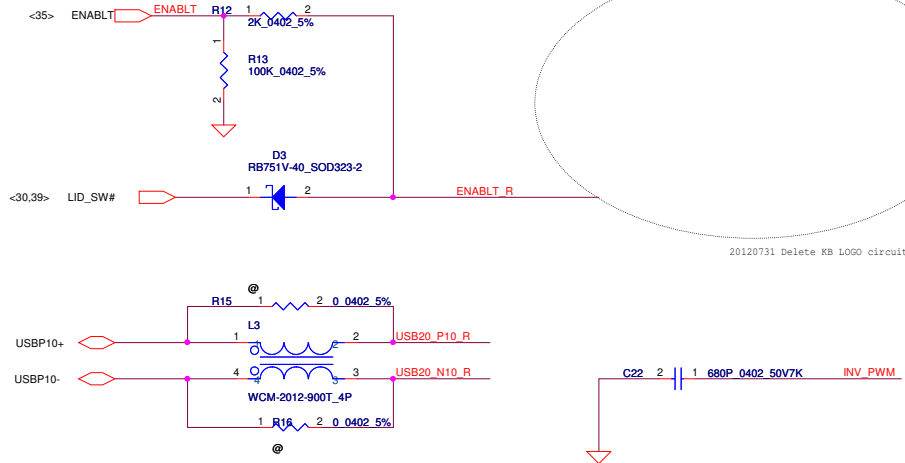
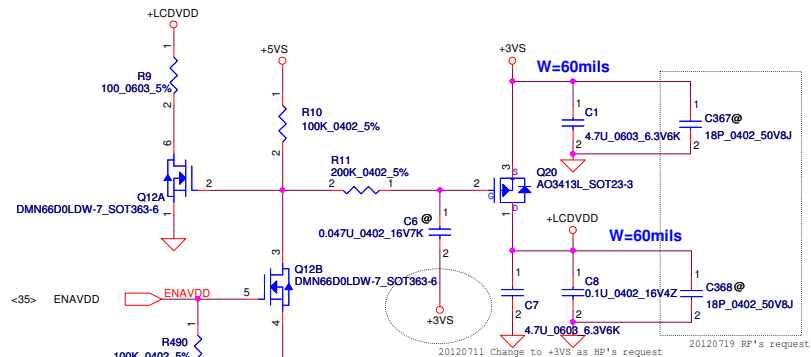


Fixed Signals				Muxed Signals		Fixed Signals						Muxed Signals		Fixed Signals			
USB3_1	USB3_2	USB3_5	USB3_6	PCIE_1	PCIE_2	PCIE_3	PCIE_4	PCIE_5	PCIE_6	PCIE_7	PCIE_8	SATA_4	SATA_5	SATA_0	SATA_1	SATA_2	SATA_3
				(00)	(00)							(00)	(00)				
				USB3_3	USB3_4							PCIE_1	PCIE_2				

[illegible]

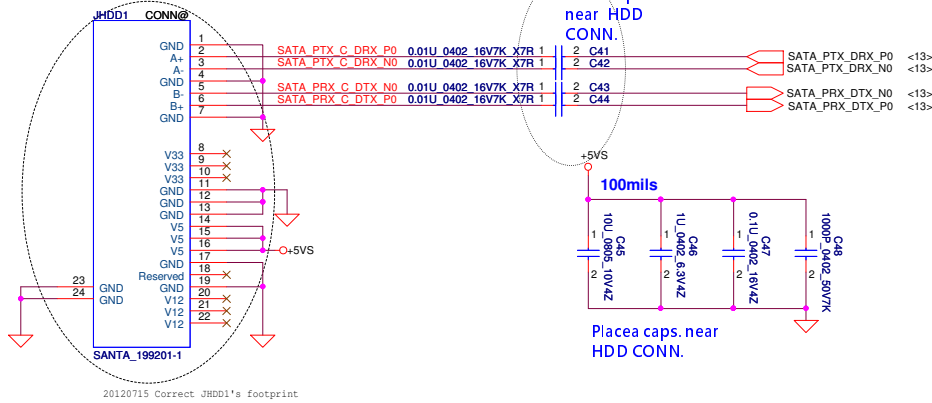
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Issued Date	2012/06/11	Deciphered Date	2013/06/11	Title		
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				Document Number LA-9371P		
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LCD POWER CIRCUIT

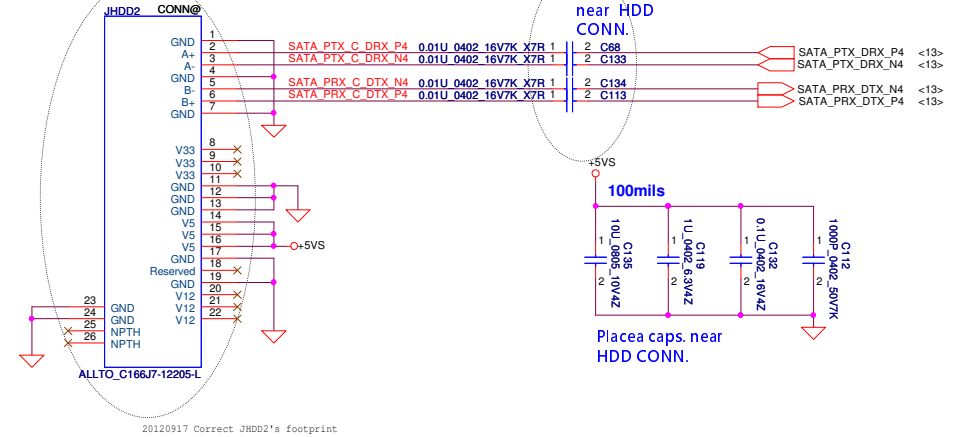


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Issued Date	2012/06/11	Deciphered Date	2013/06/11	Title	eDP/LVDS CONN & Camera	
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				LA-9371P		
				Date: Friday, September 28, 2012		Sheet 22 of 53

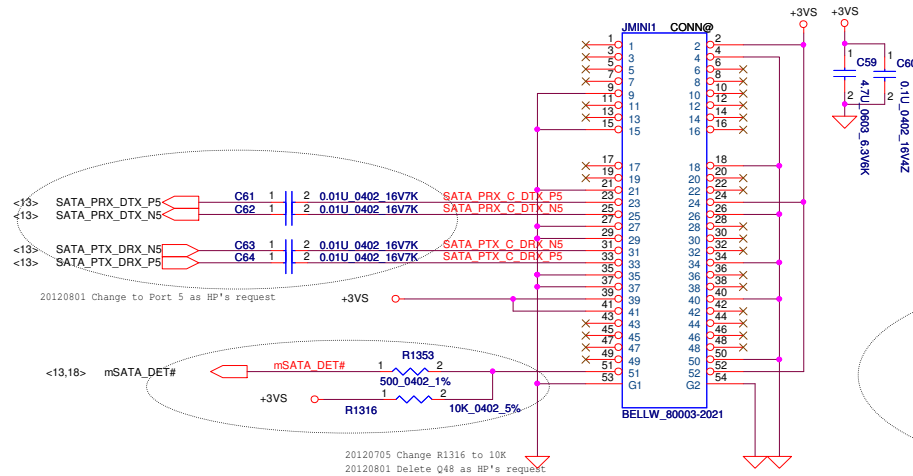
SATA Primary HDD CONN.



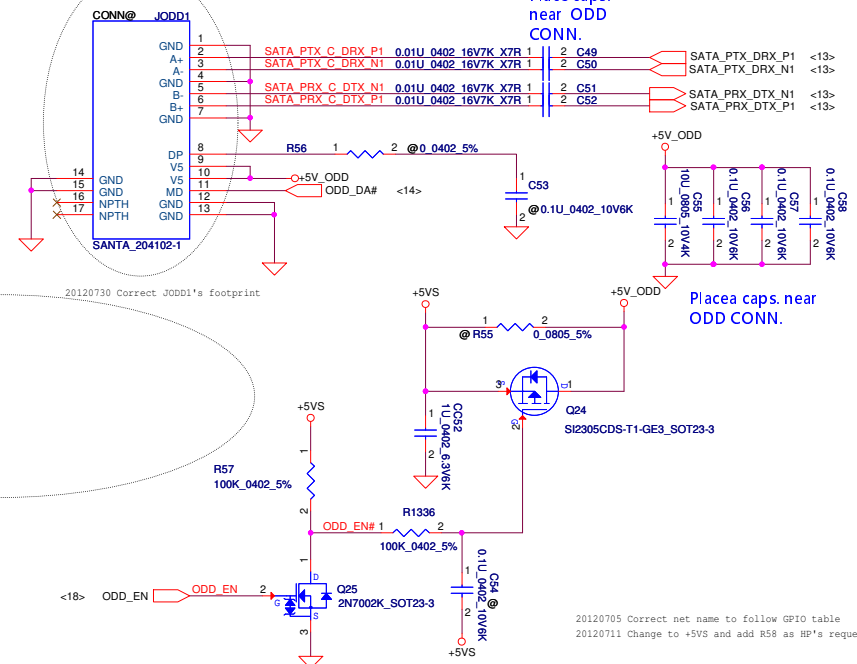
SATA Second HDD CONN.



mSATA Conn.

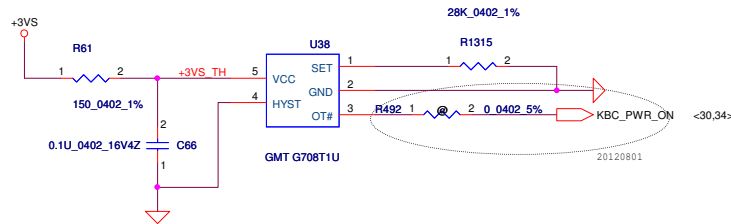
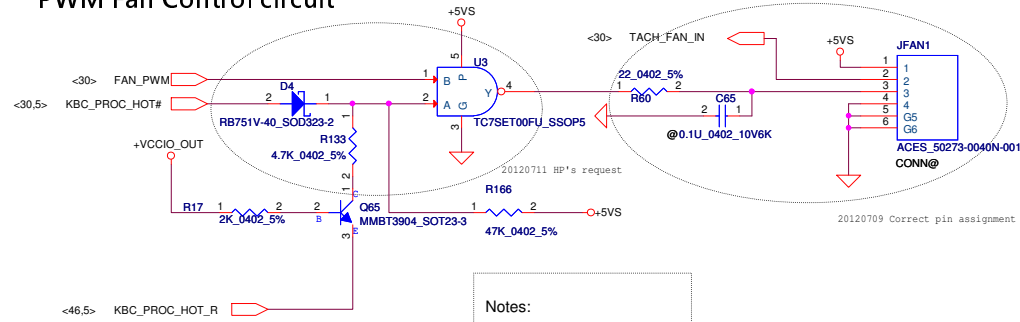


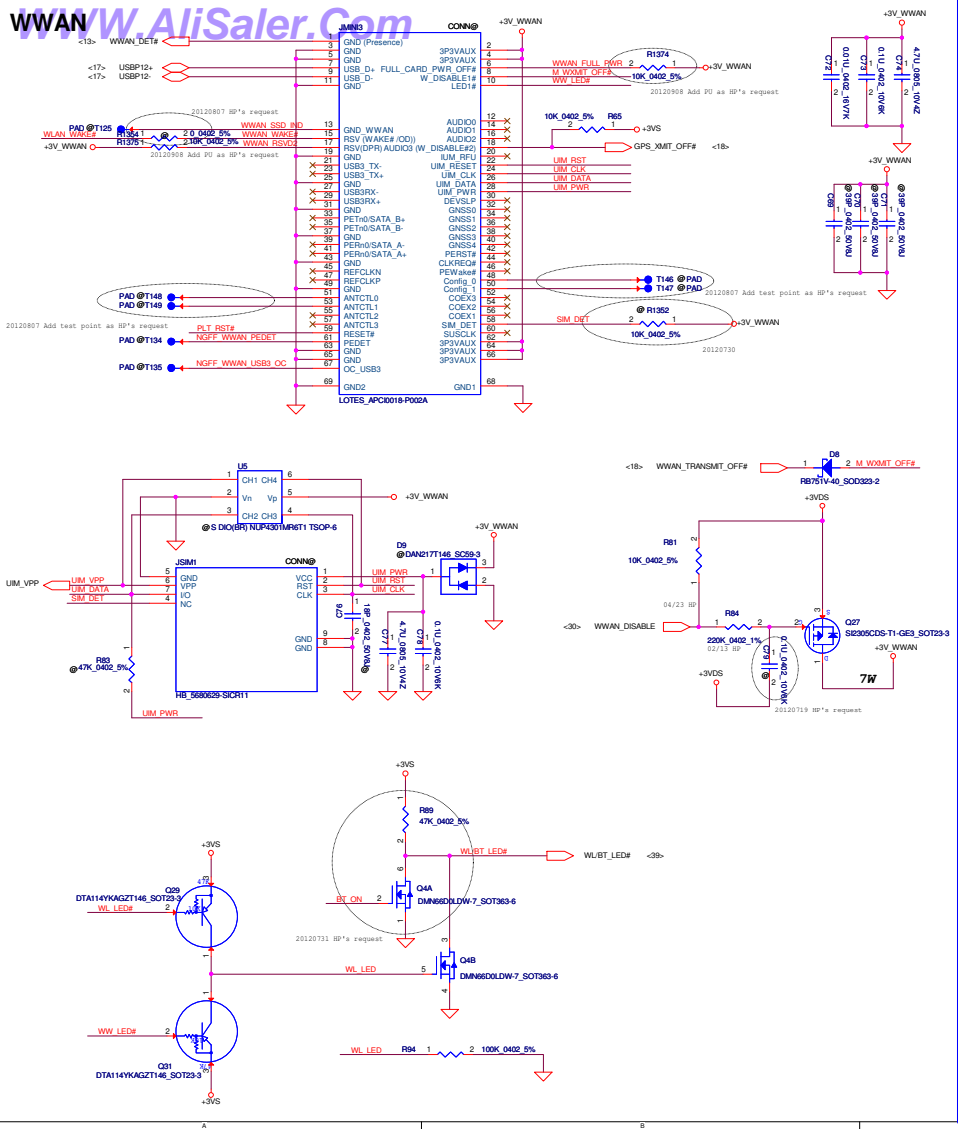
SATA ODD CONN.



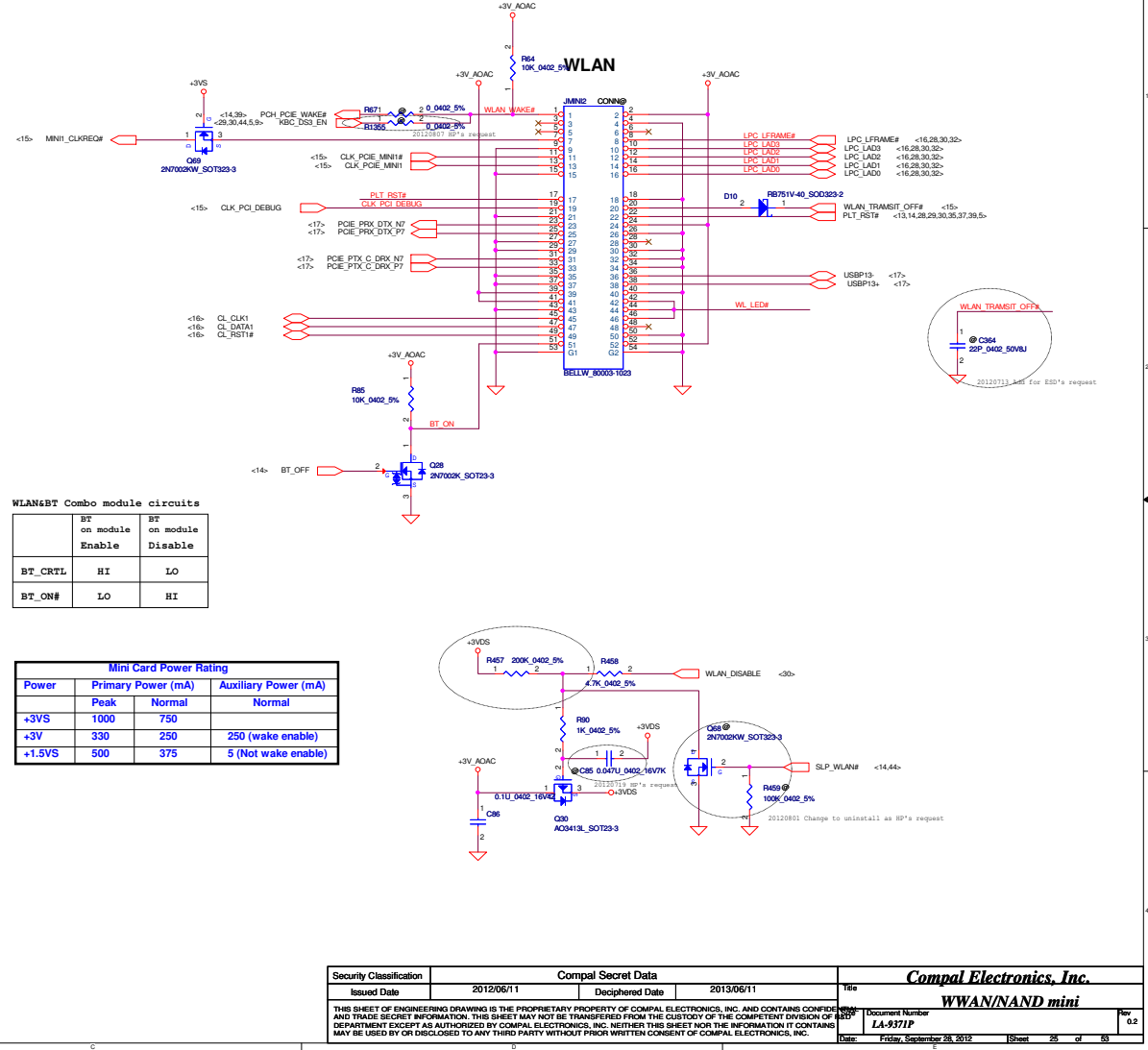
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/06/11	Deciphered Date	2013/06/11	Title	IBEX-M(IU/6)-HDA/JTAG/SATA
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				Date:	Friday, September 28, 2012
				Sheet	23 of 53

PWM Fan Control circuit





WLAN



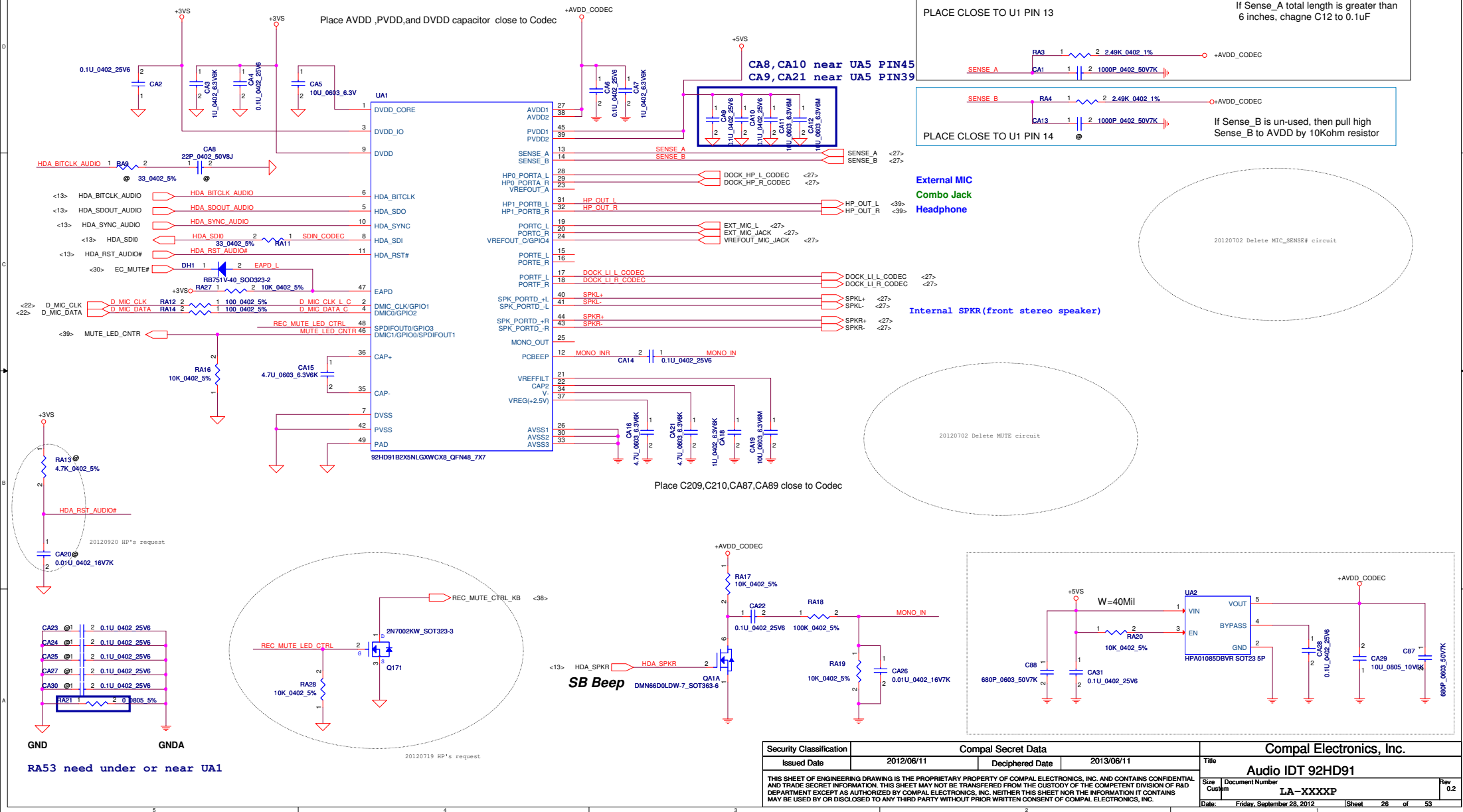
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	HI	LO
BT_ON#	LO	HI

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

Security Classification		Compal Secret Data		Title	
Issued Date	2012/06/11	Deciphered Date	2013/06/11	Docu	WWAN/NAND mini
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Date	Friday, September 28, 2012	Sheet	25	of	63

Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals





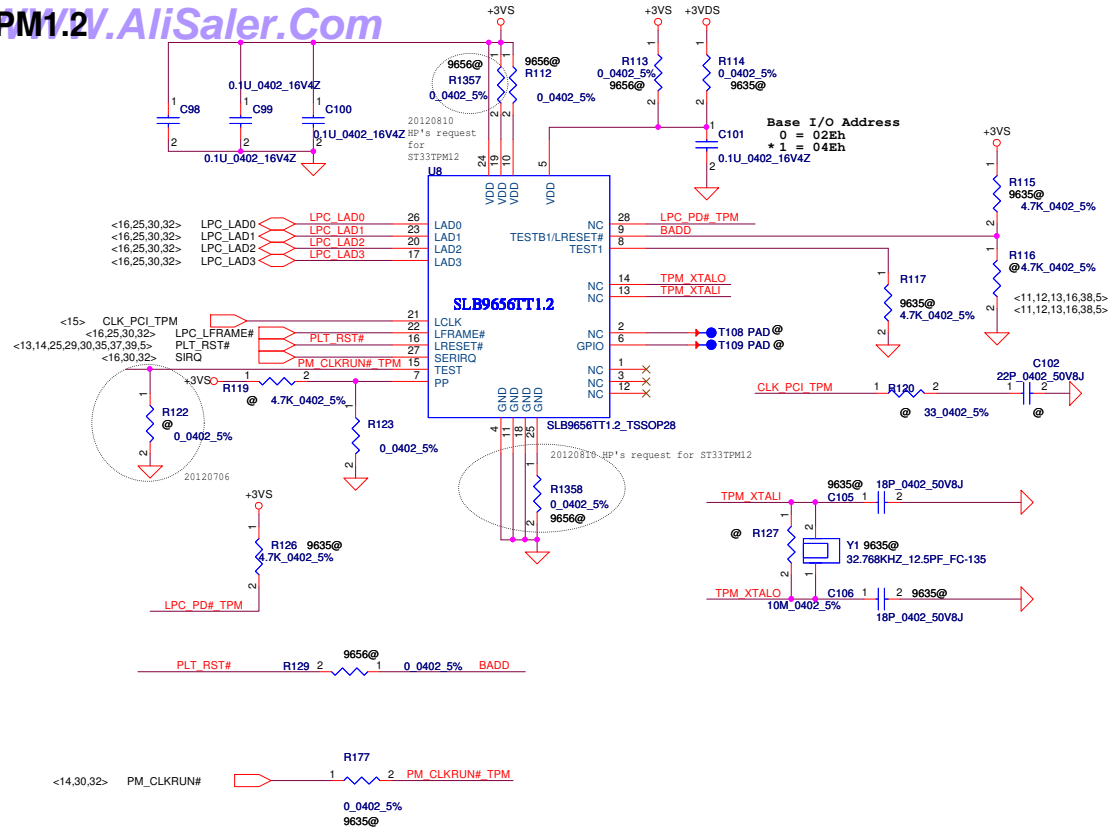
DOCK Audio



20120713 Move to S/E

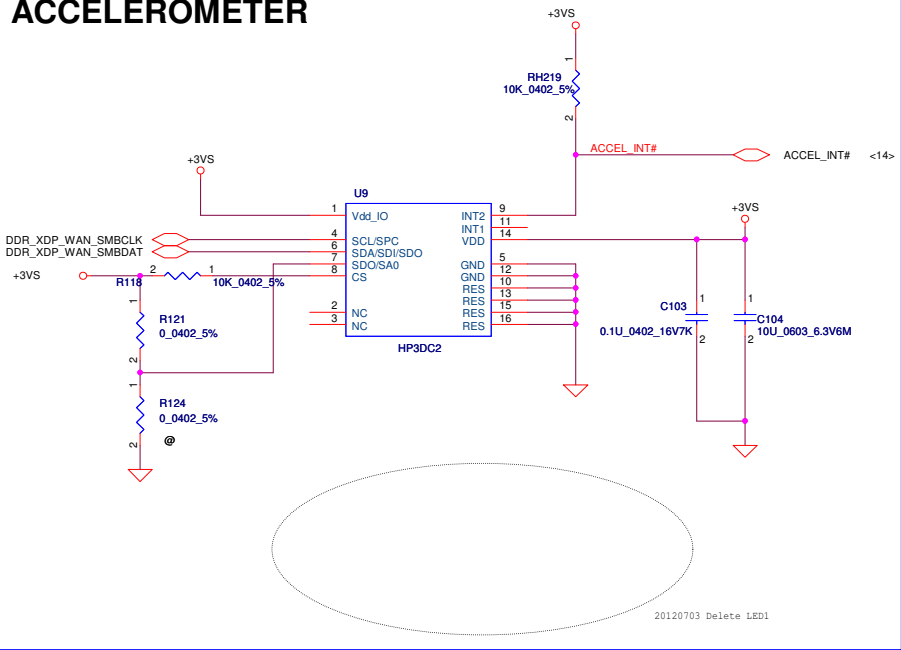


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Issued Date	2012/06/11	Deciphered Date	2013/06/11	Title	Audio SPK Conn/Jack/MIC	
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				C	LA-9371P	0.2
				Date:	Friday, September 26, 2012	Sheet 27 of 53

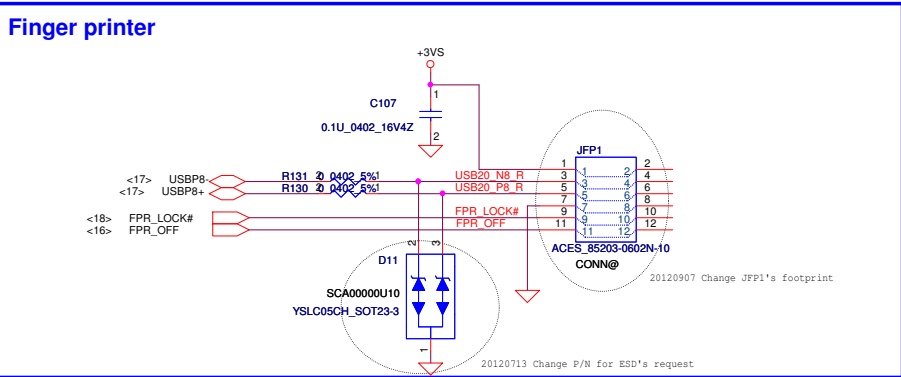


TPM	BOM Option (Not Install)
SLB9635	R112, R113, R129
SLB9656	R114, R115, R117, R126, R177, C105, C106, Y1
ST33TPM12	R113, R129, R114, R115, R117, R126, R177, R1357, R1358, R127, R122, R116, R120, C102, C101, C105, C106, Y1

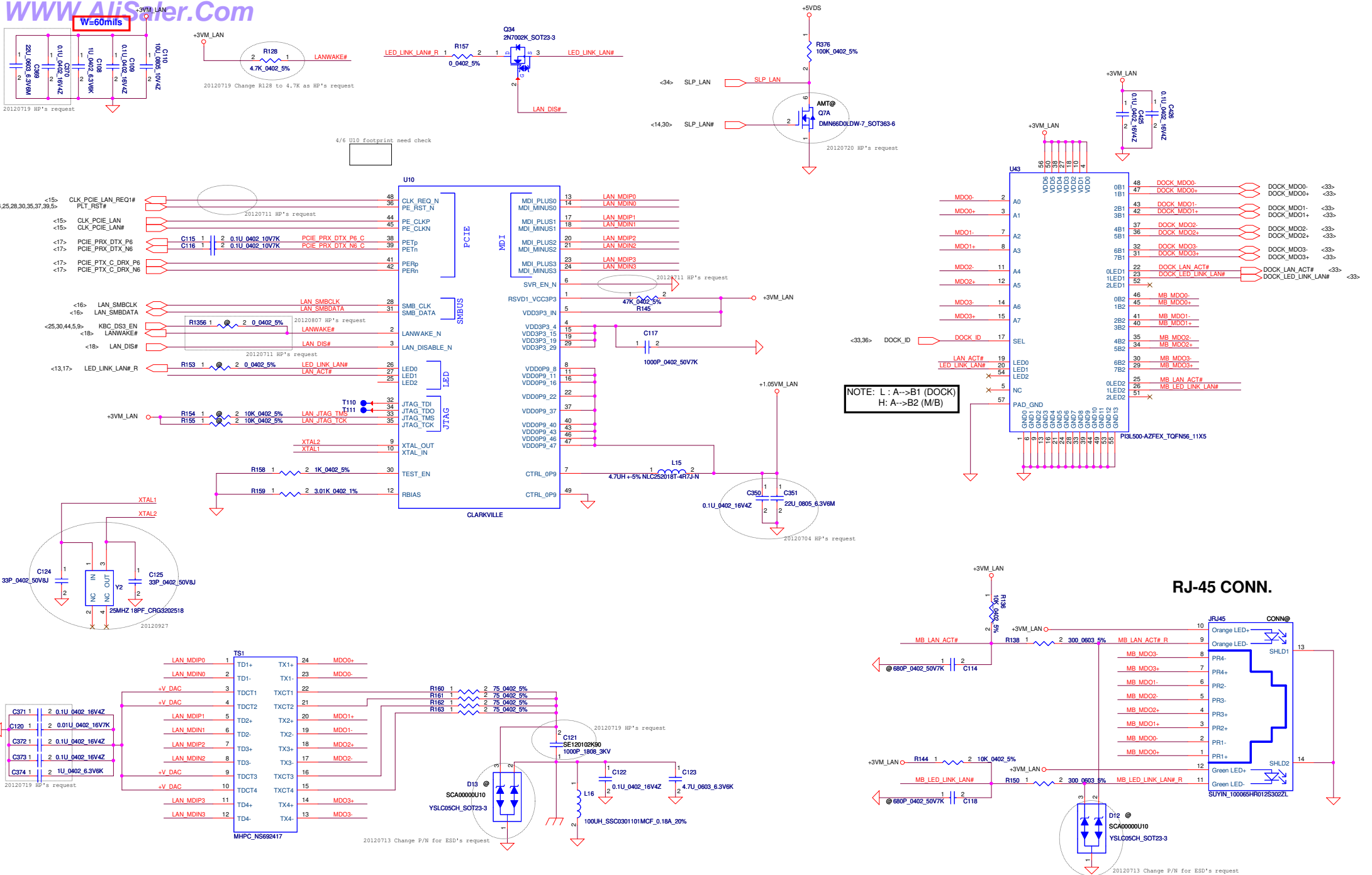
ACCELEROMETER



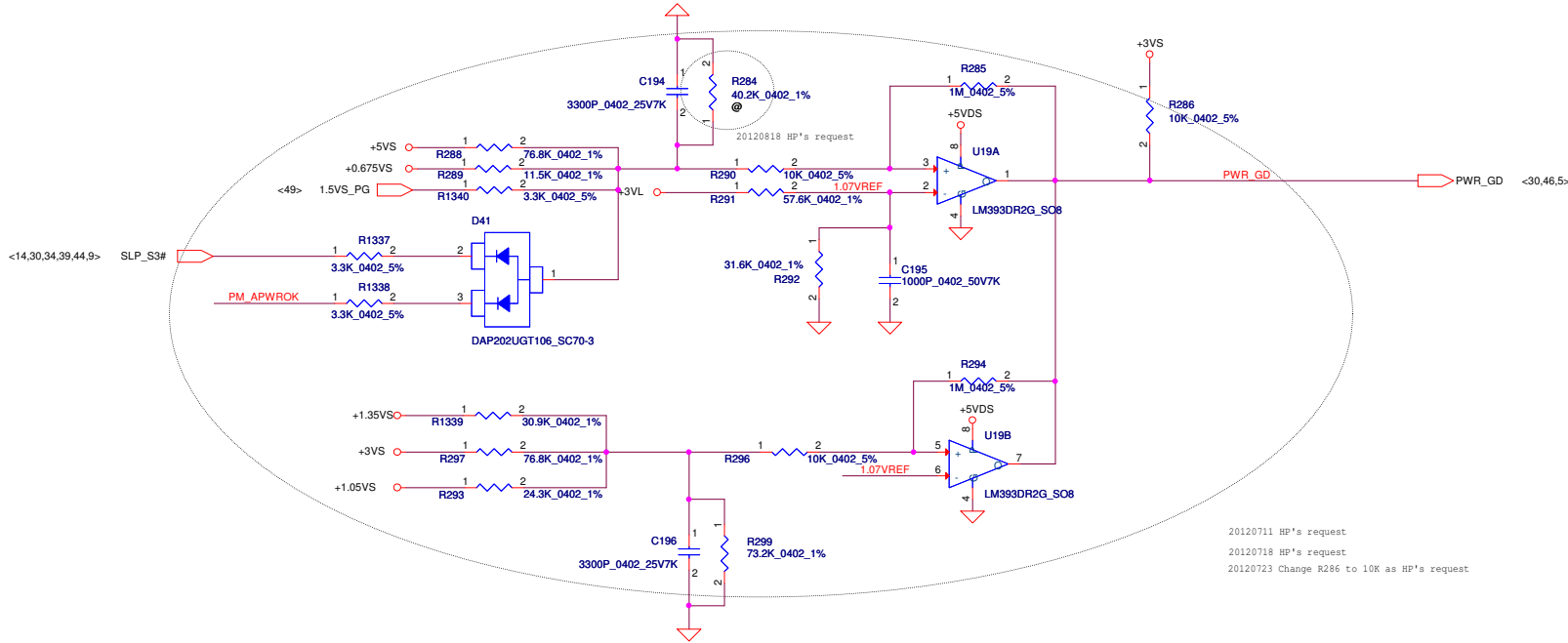
Finger printer



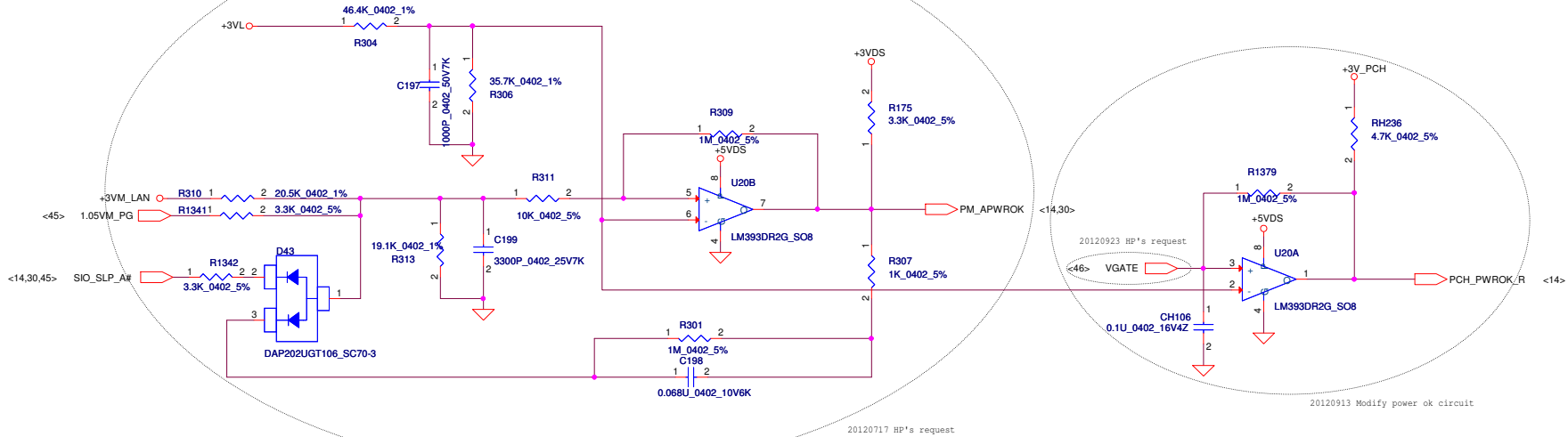
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Issued Date	2012/06/11	Deciphered Date	2013/06/11	Title	
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Date:				Friday, September 28, 2012	Sheet 28 of 53



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Date:	Friday, September 28, 2012	Sheet	29	of 53	



20120711 HP's request
20120718 HP's request
20120723 Change R286 to 10K as HP's request

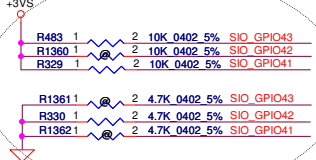
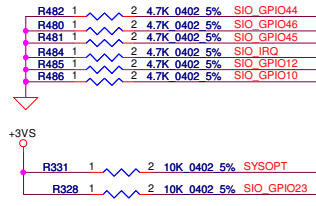
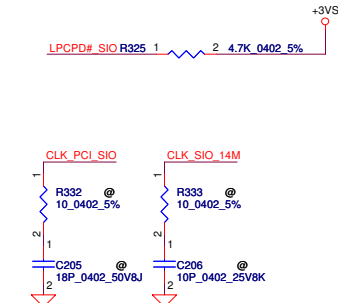
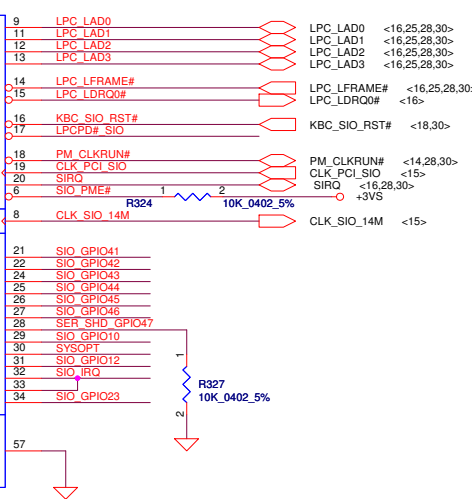
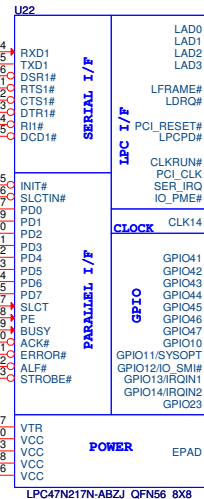
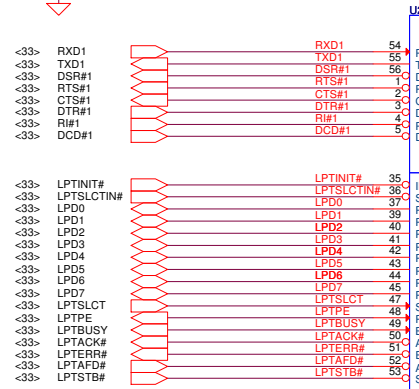
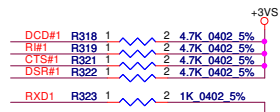
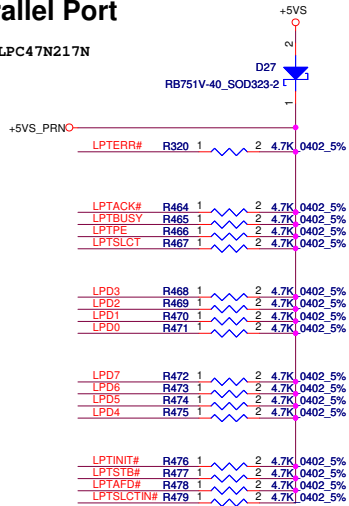


20120913 Modify power ok circuit

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				Date:	Friday, September 28, 2012
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Parallel Port

TO LPC47N217N



20120720 System ID for HP's request
20120731 System ID for HP's request
20120821 Add R for 2019M & 4019M option

Platform IDs (Super I/O GPIOs)

PLT_ID1	PLT_ID2	PLT_ID3	SYSTEM ID	Series	CPU	Dock	COMMON BIOS
GPIO43	GPIO42	GPIO41					
1	0	1	Afterburner 17" 4 DIMM	W	Haswell	Common	8
1	1	1	Afterburner 17" 2 DIMM	W	Haswell	Common	8

DOCK CONN. 184PIN

DOCKING CONNECT

- (1) PCI Express x1 channels
- (2) P8/2 Interfaces
- (2) USB 2.channels
- (2) SATA Channels
- (2) Display Port Channels
- (1) Serial Port
- (1) Parallel Port
- (1) Line In
- (1) Line Out
- (1) RJ45 (10/100/1000)
- (1) VGA
- (1) 2 LAN indicator LED's
- (1) Power Button
- (1) I2C interface



L30ESD24VC3-2_SOT23-3

12A

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G1

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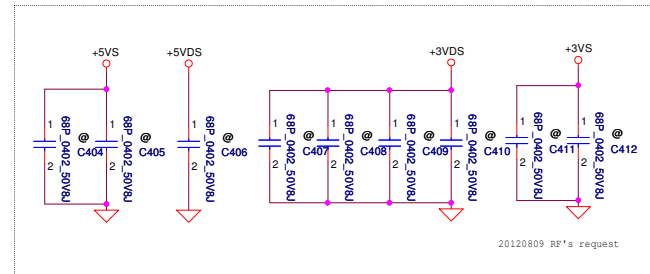
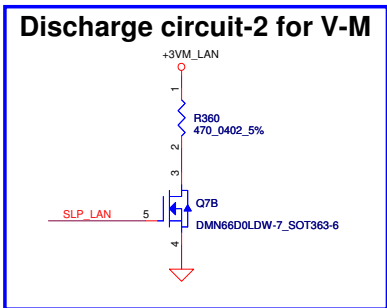
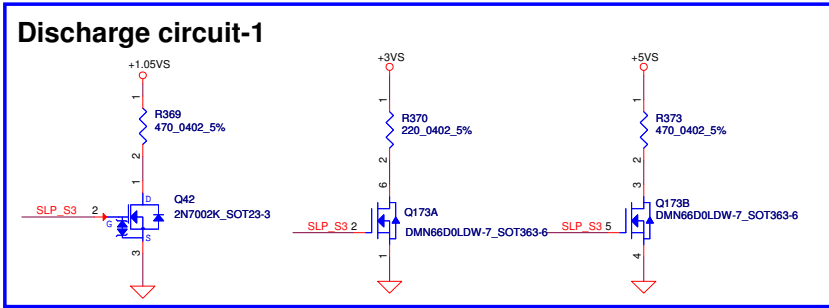
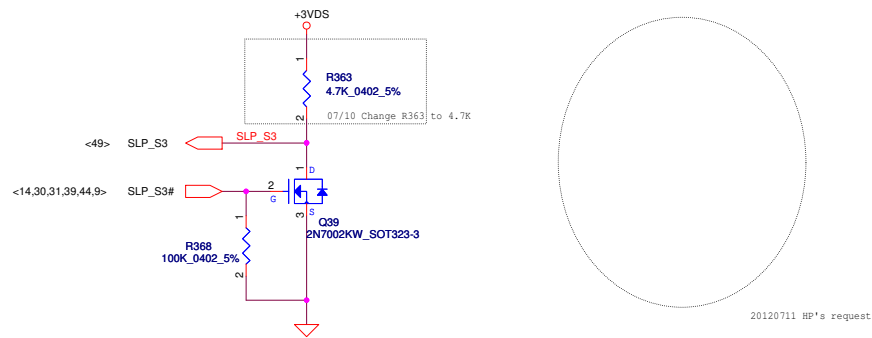
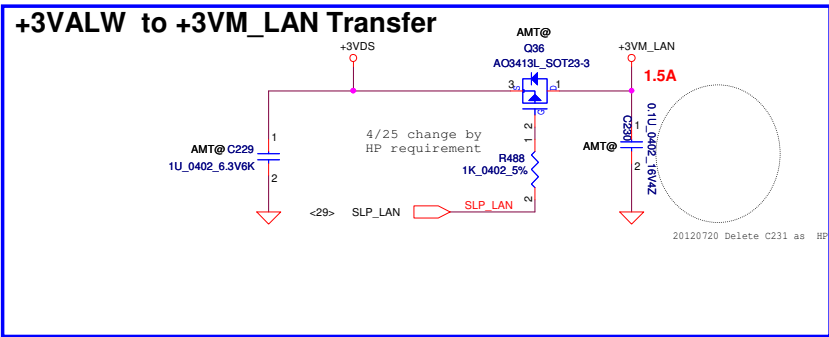
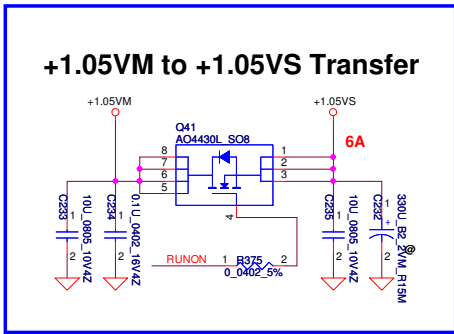
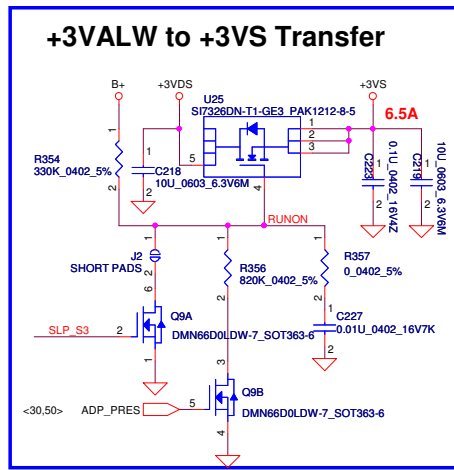
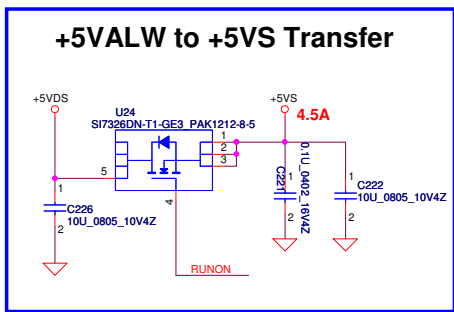
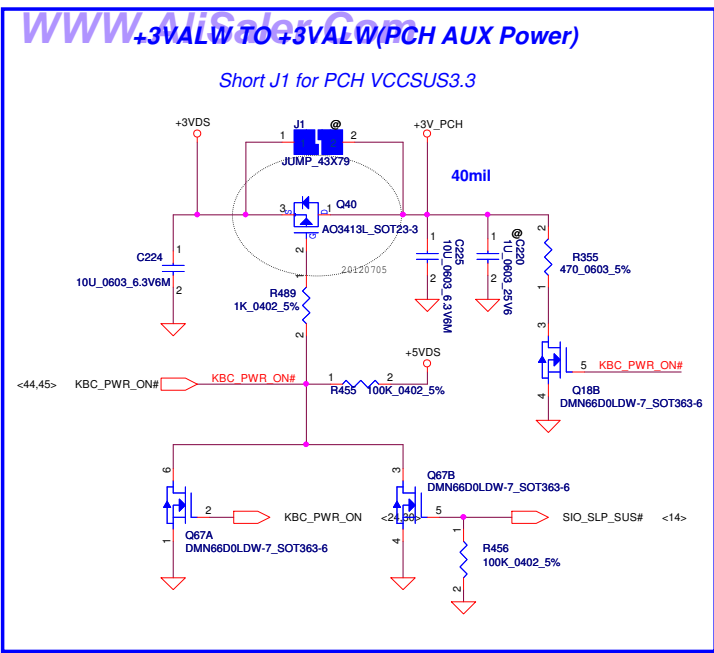
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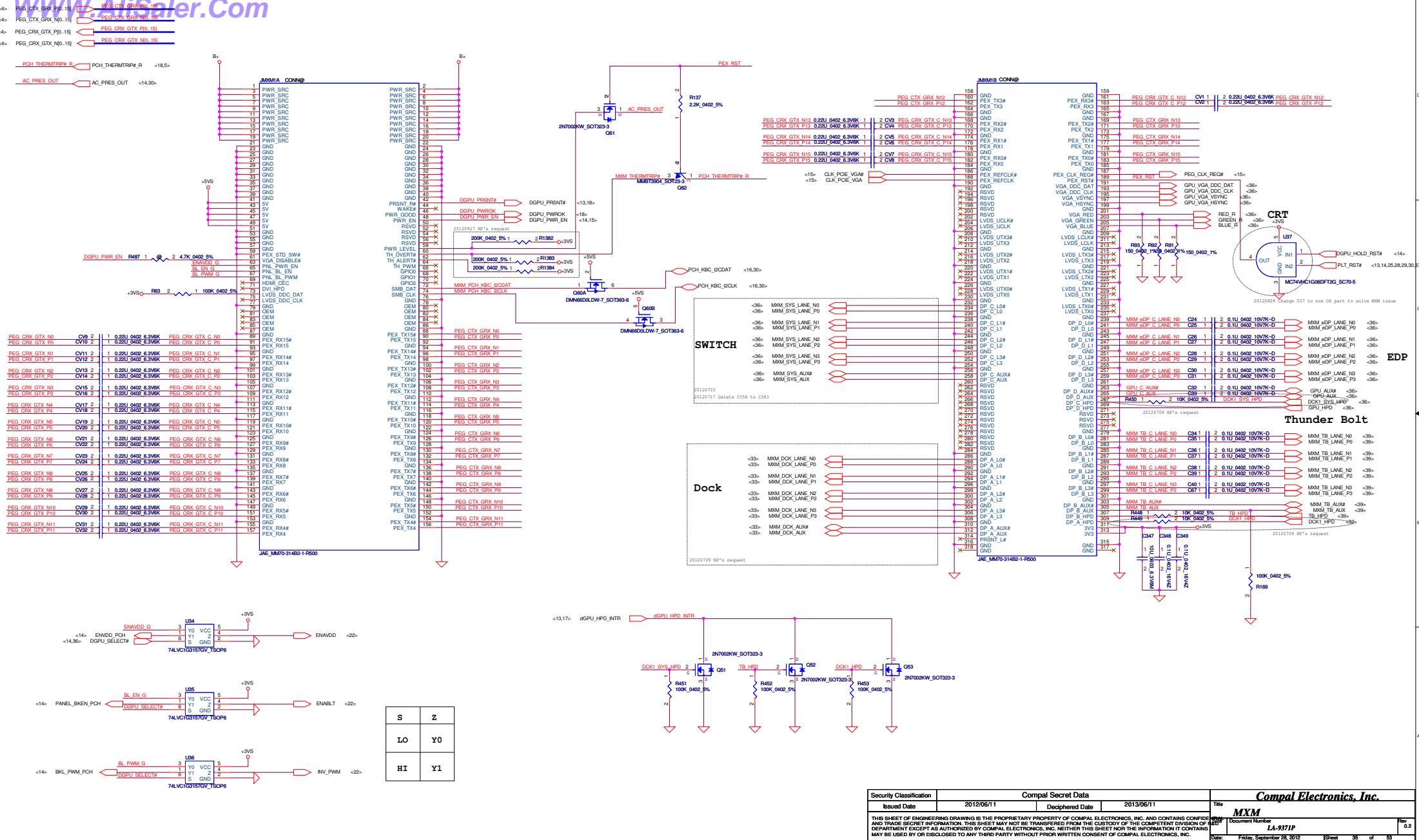
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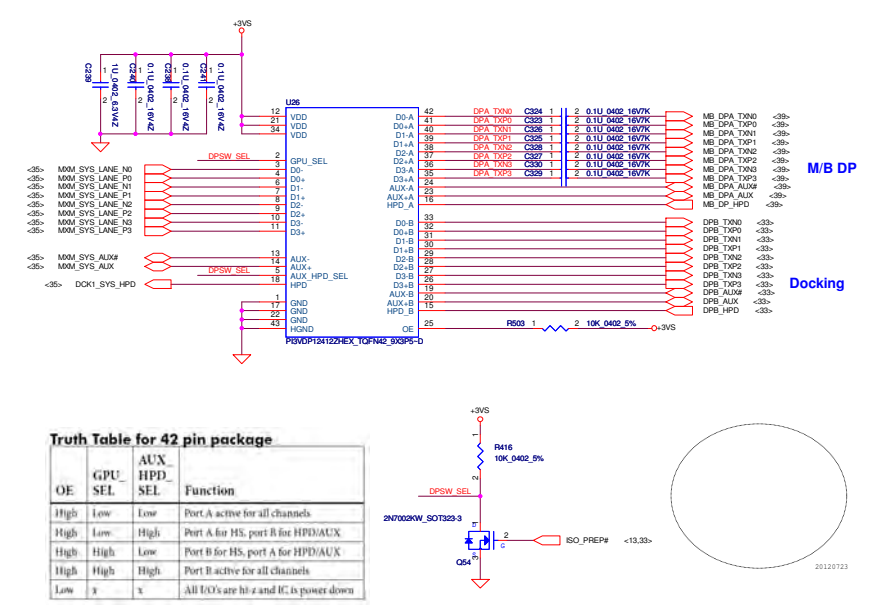
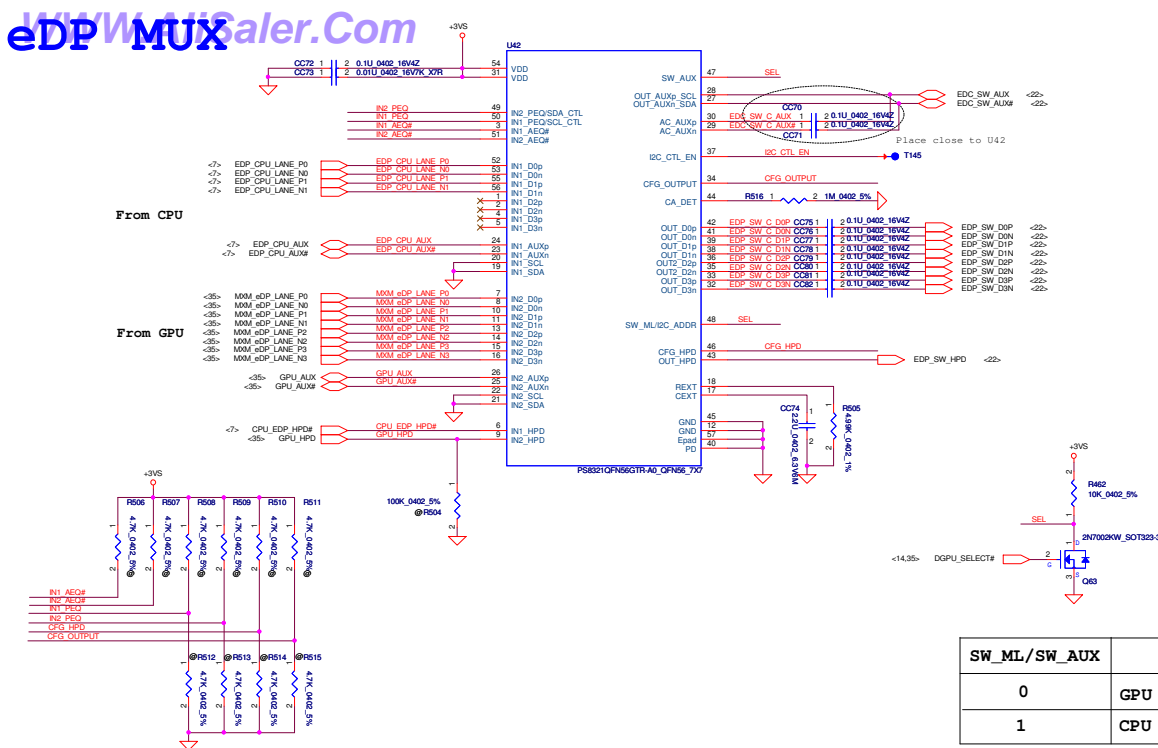




S	Z
LO	Y0
HI	Y1

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DP Switch

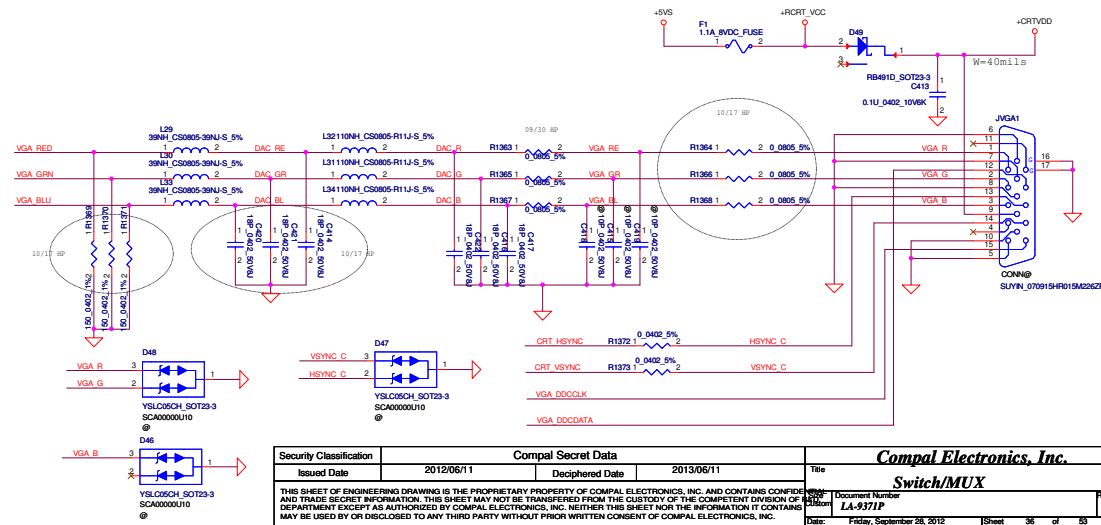
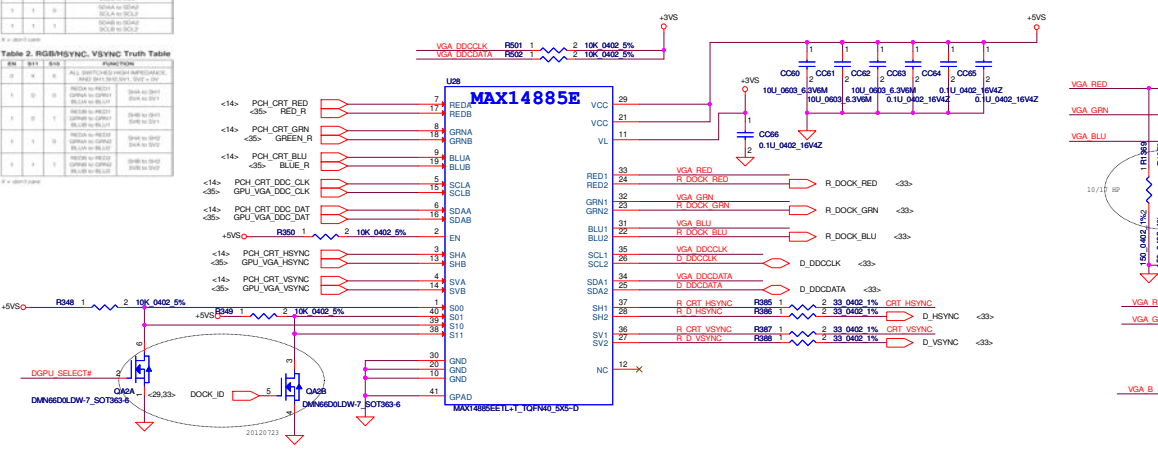



OE	GPU_SEL	AUX_HPD_SEL	Function
High	Low	Low	Port A active for all channels
High	Low	High	Port A for HS, port B for HPD/AUX
High	High	Low	Port B for HS, port A for HPD/AUX
High	High	High	Port B active for all channels
Low	x	x	All I/O's are hi-z and IC is power down

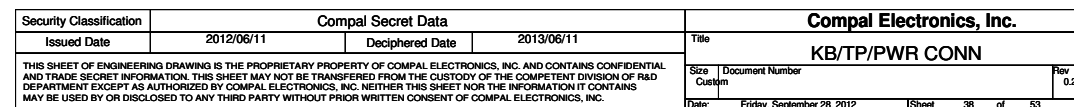
SW_ML/SW_AUX	
0	GPU
1	CPU

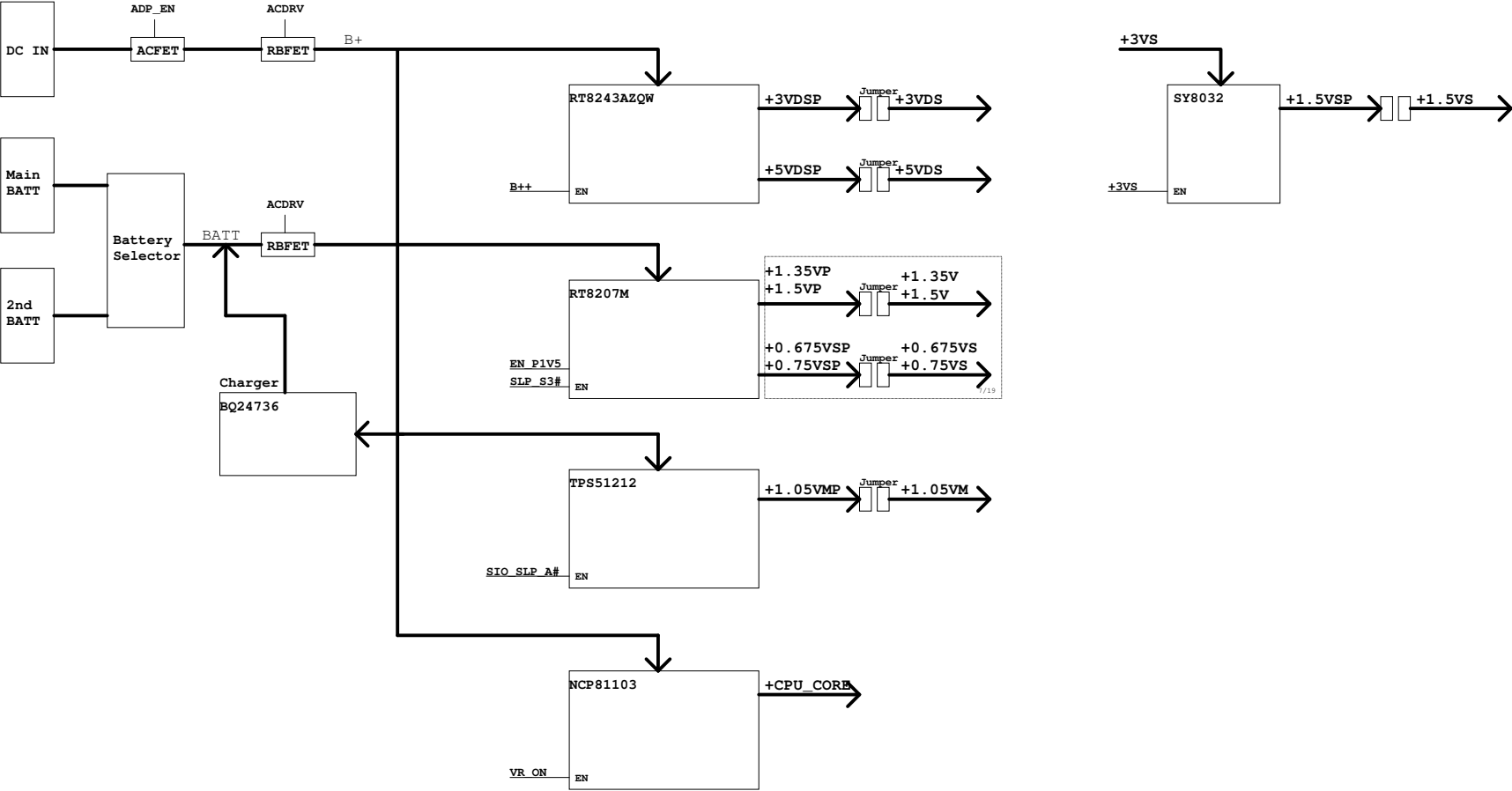
EN	SD1	SD0	FUNCTION
0	x	0	ALL SWITCHES HIGH - FREQUENCY
1	0	0	SDWA to SDA1 SCLA to SCL1
1	0	1	SDWB to SDA1 SCLB to SCL1
1	1	0	SDWA to SDA2 SCLA to SCL2
1	1	1	SDWB to SDA2 SCLB to SCL2

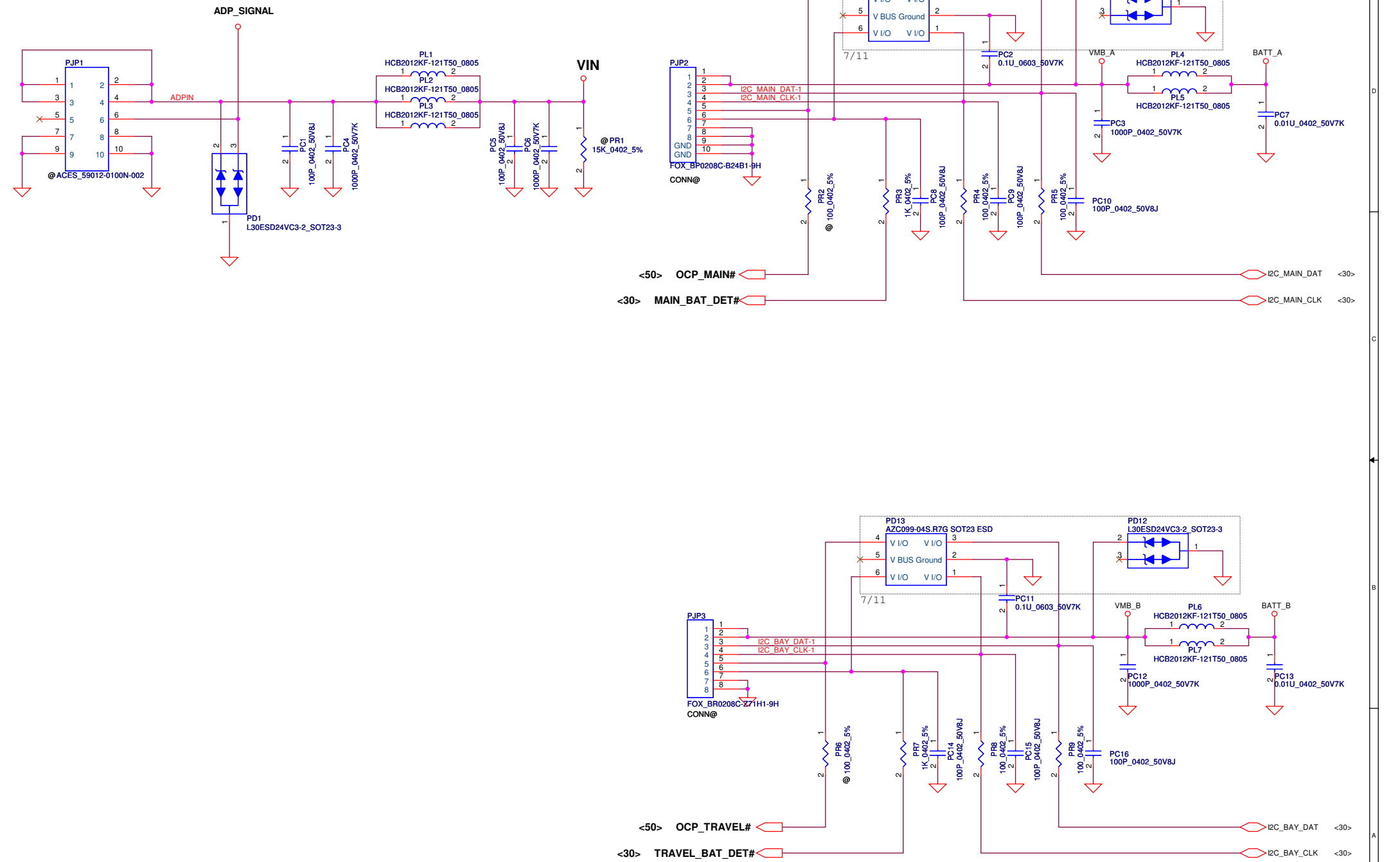
EN	Q11	S-0	Function
0	X	X	All Switched input PERFORMANCE, AND S-011 S-011, S-02 = 0V
1	0	0	RGB to RGB1 C-01A to C-01A1 B-01A to B-01A1
1	0	1	RGB to RGB1 C-01A to C-01A1 B-01B to B-01A1
1	1	0	RGB to RGB2 C-01A to C-01A2 B-01A to B-01A2
1	1	1	RGB to RGB2 C-01A to C-01A2 B-01B to B-01A2



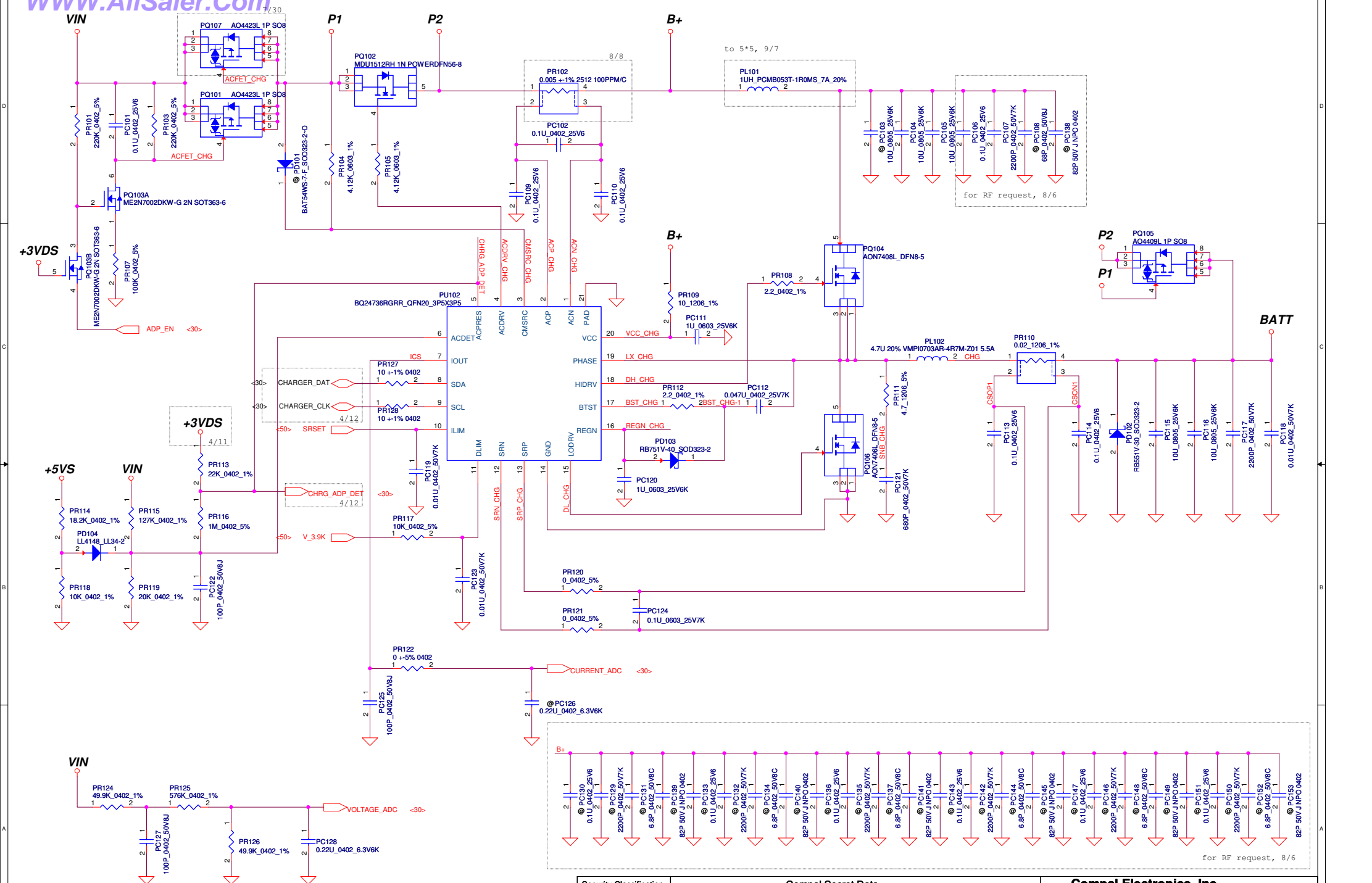
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Date: 2012/06/11			Rev: 01
Date: 2012/06/11			Sheet: 36 of 83





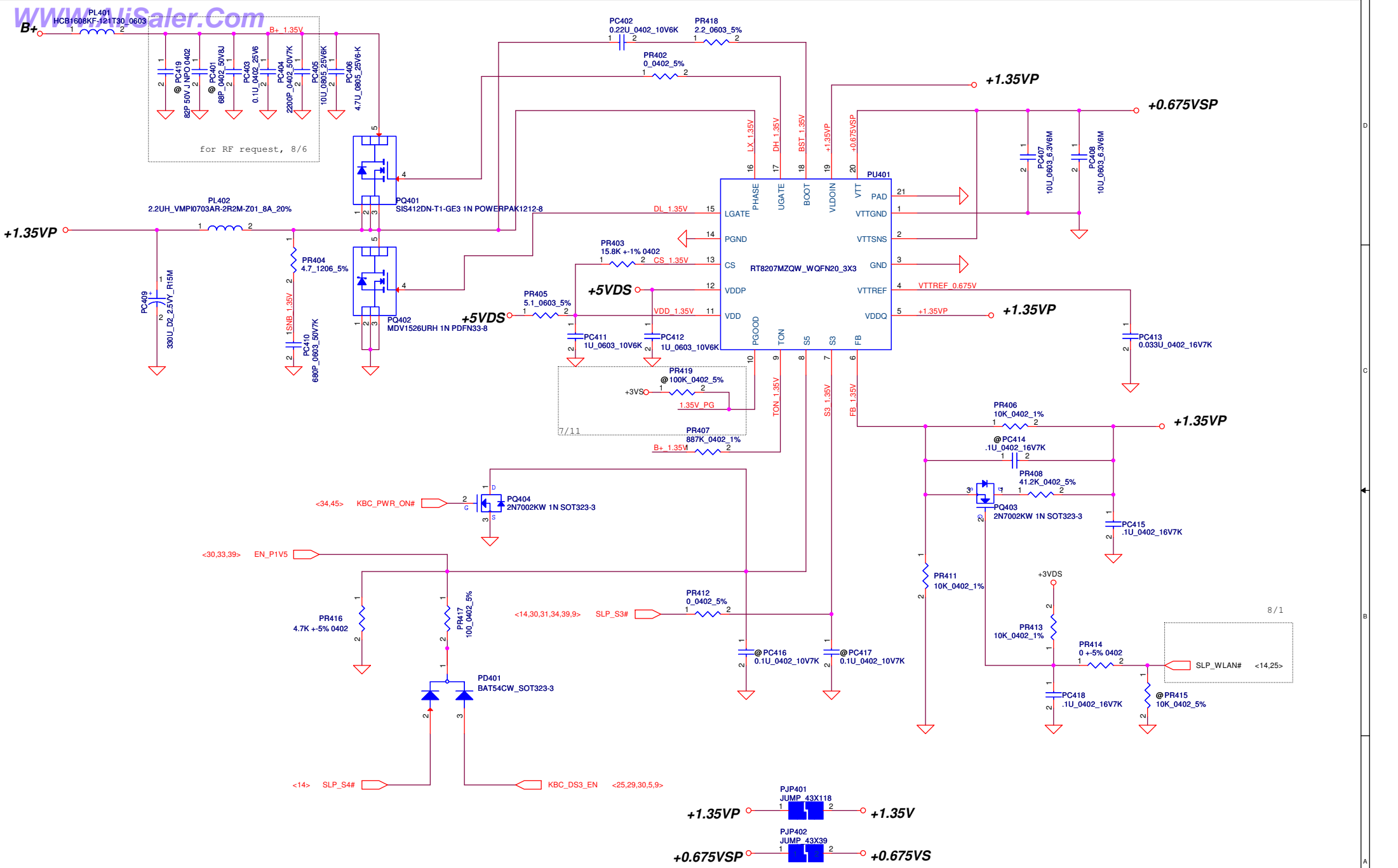


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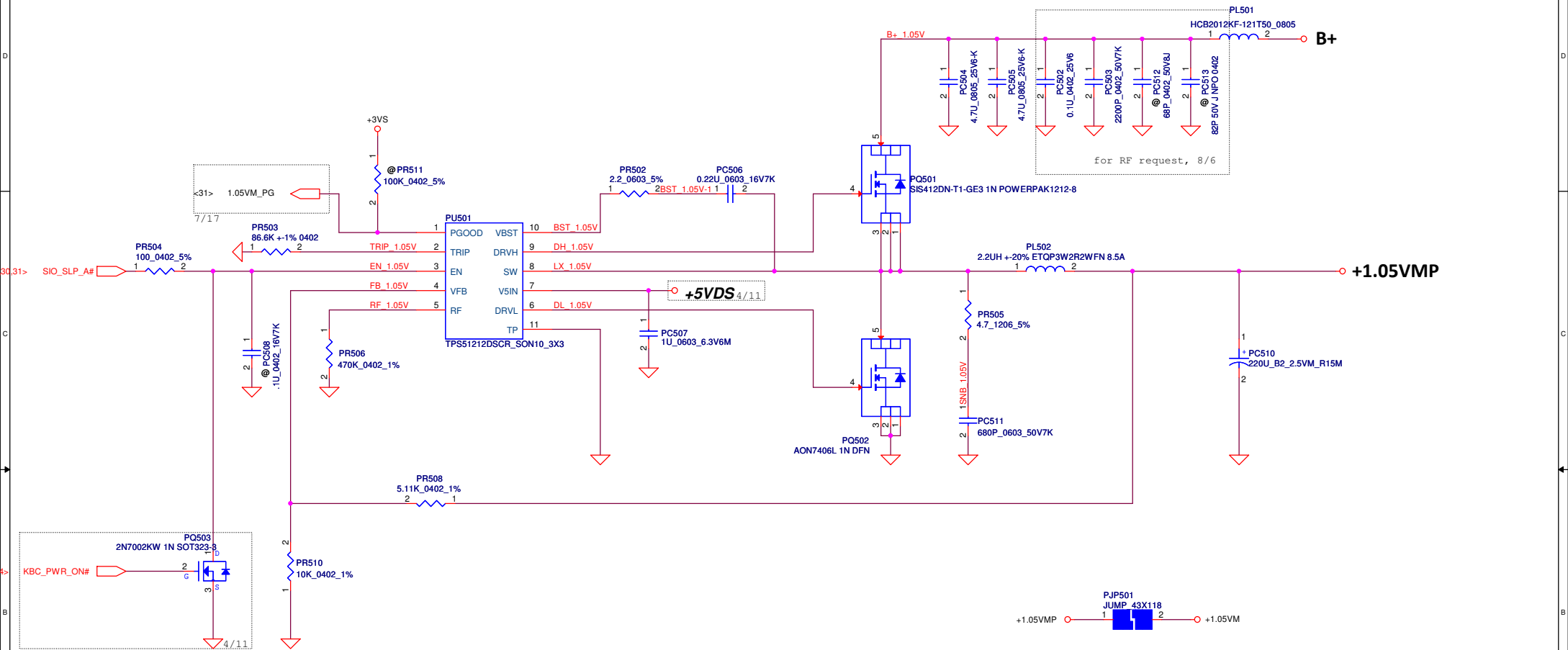


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				Date:	Friday, September 28, 2012	Sheet 42 of 53

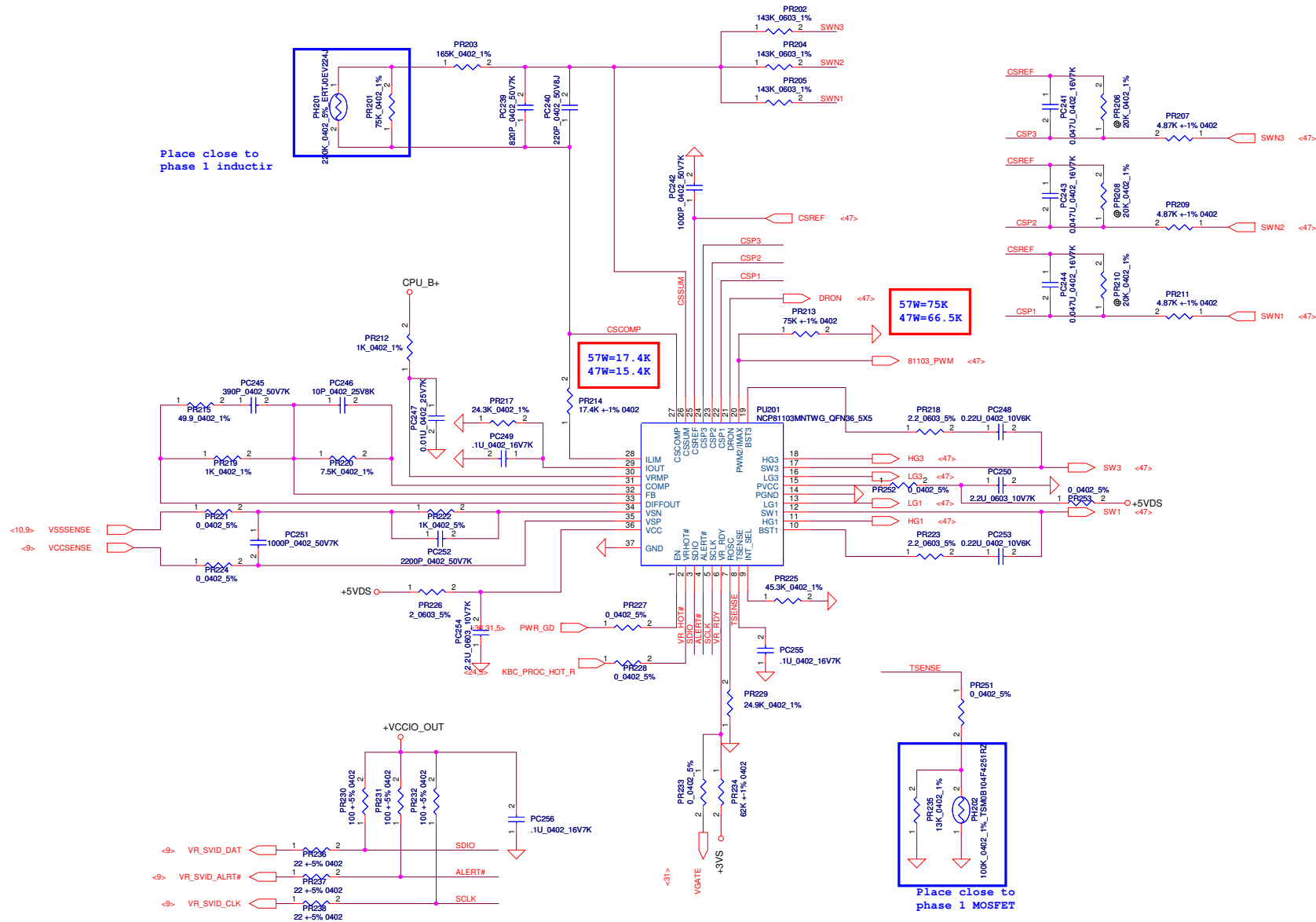
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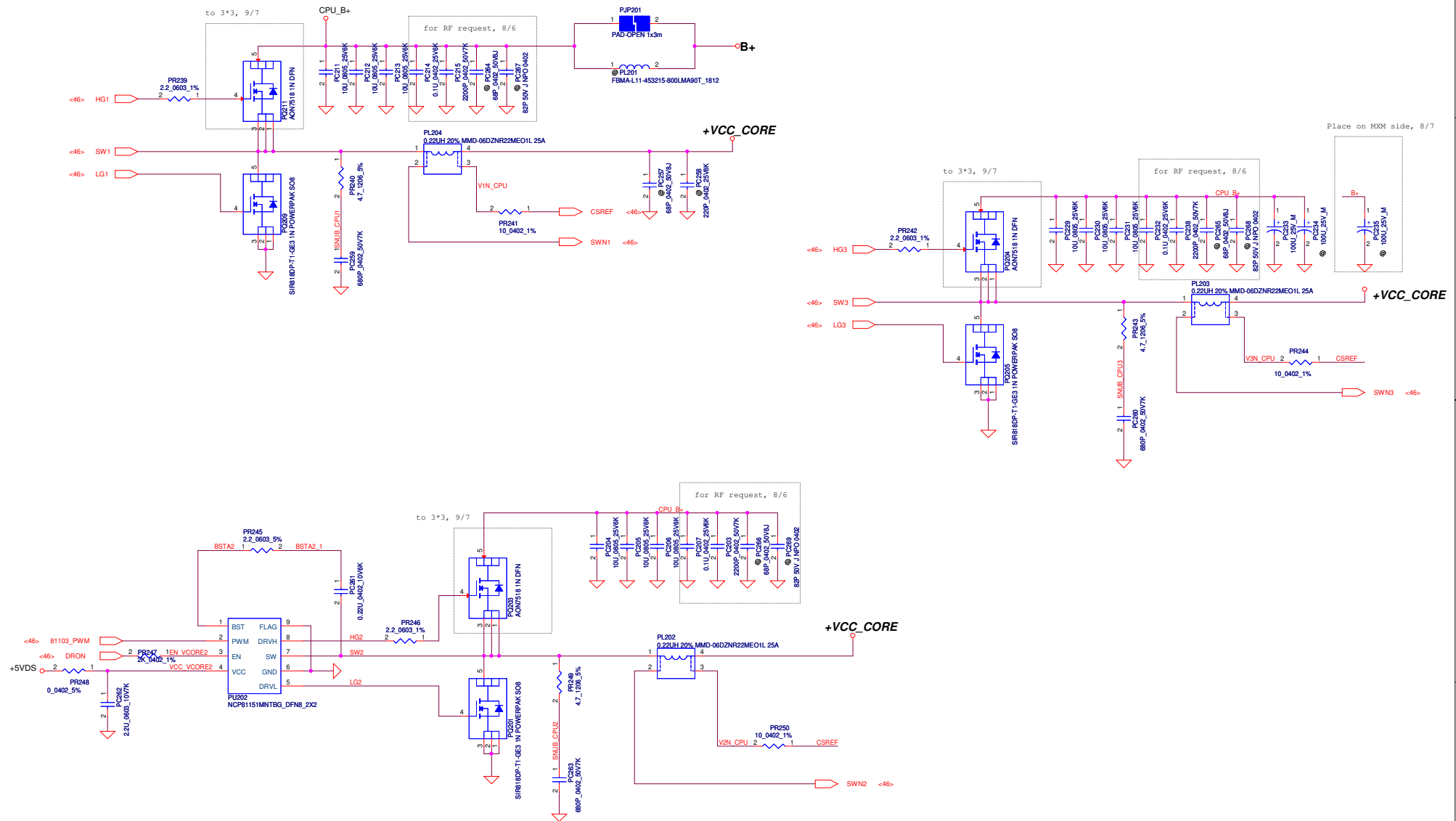
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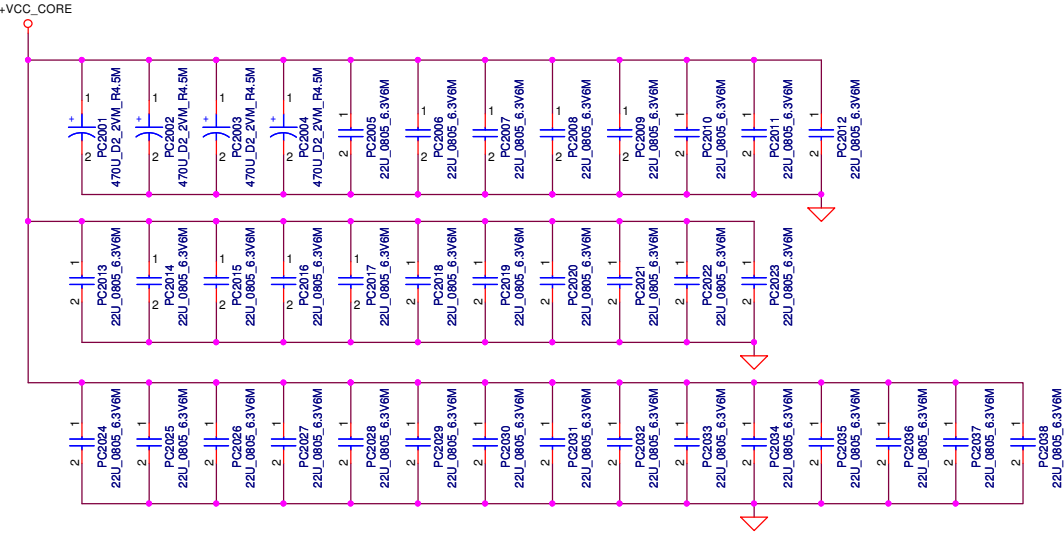
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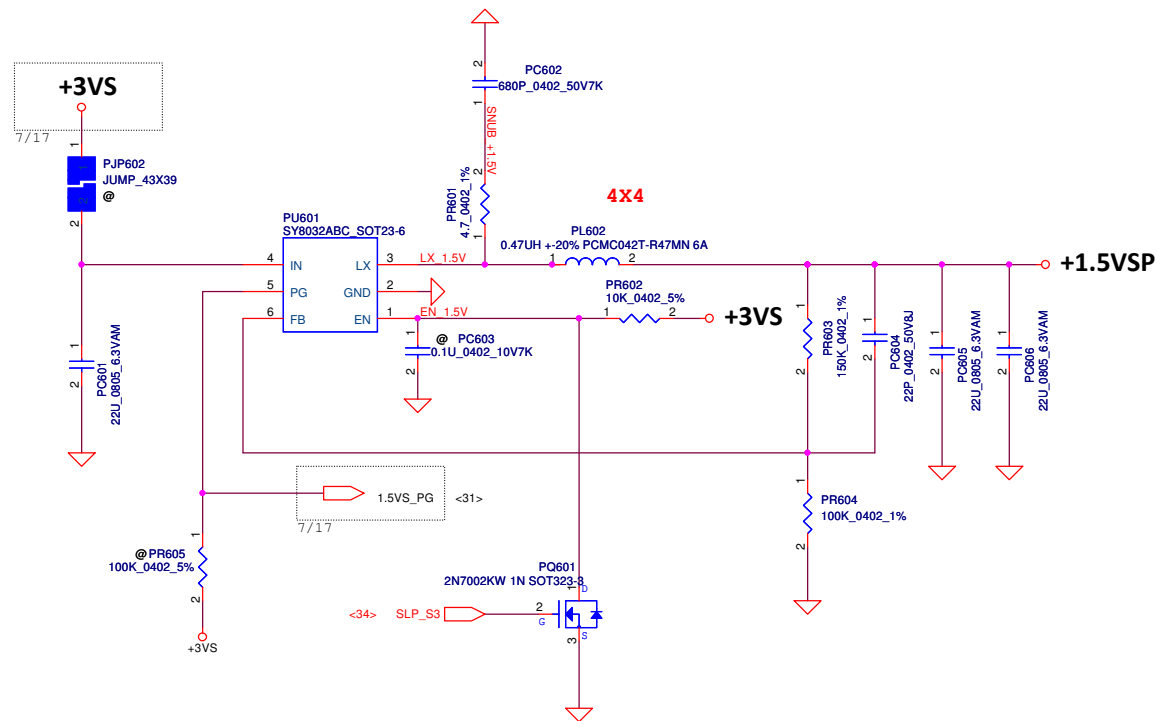
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				Sheet	46 of 53
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+VCC_CORE 4 X 470u/4m
34X 22u/0805



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				15W	0.2
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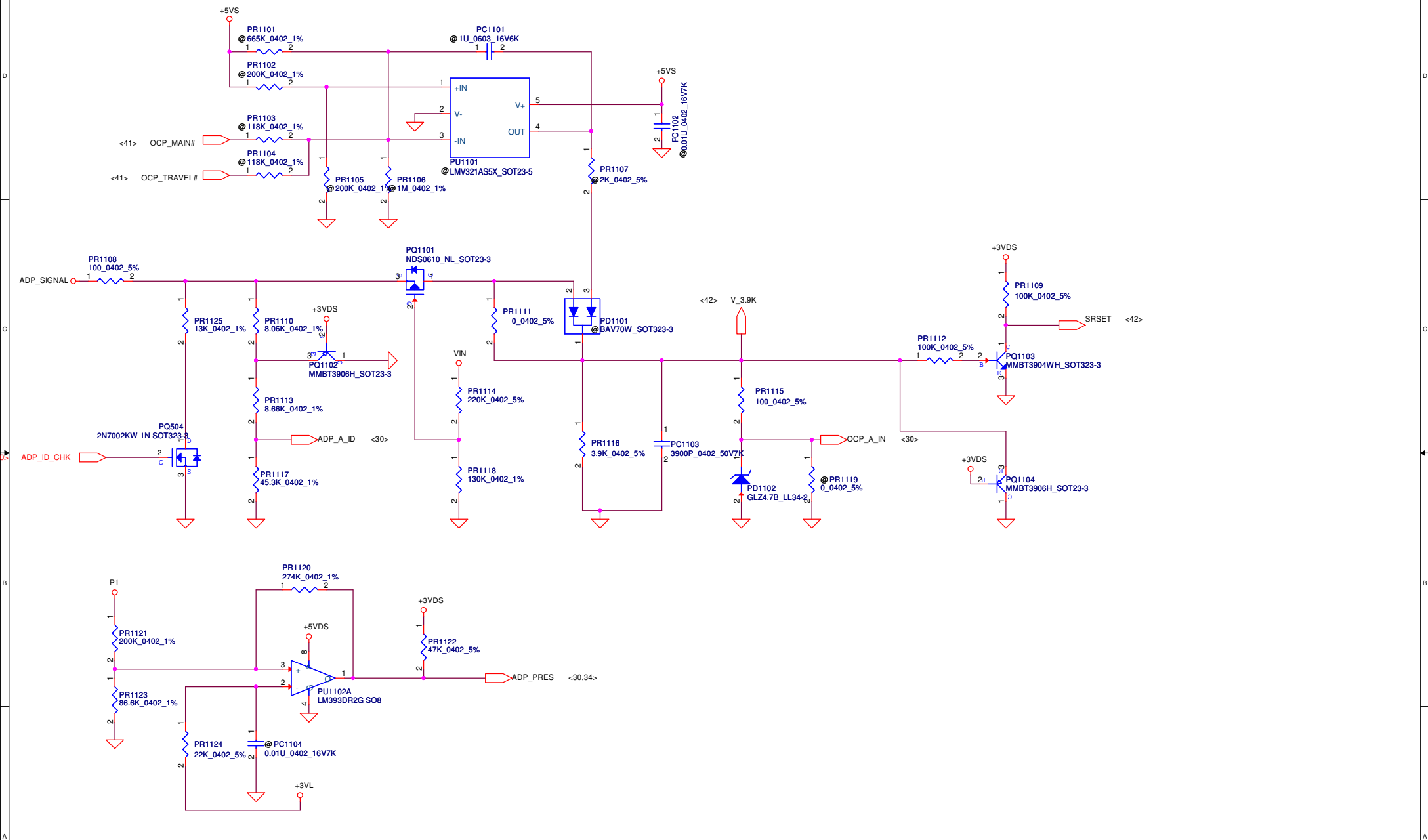


+1.5VSP

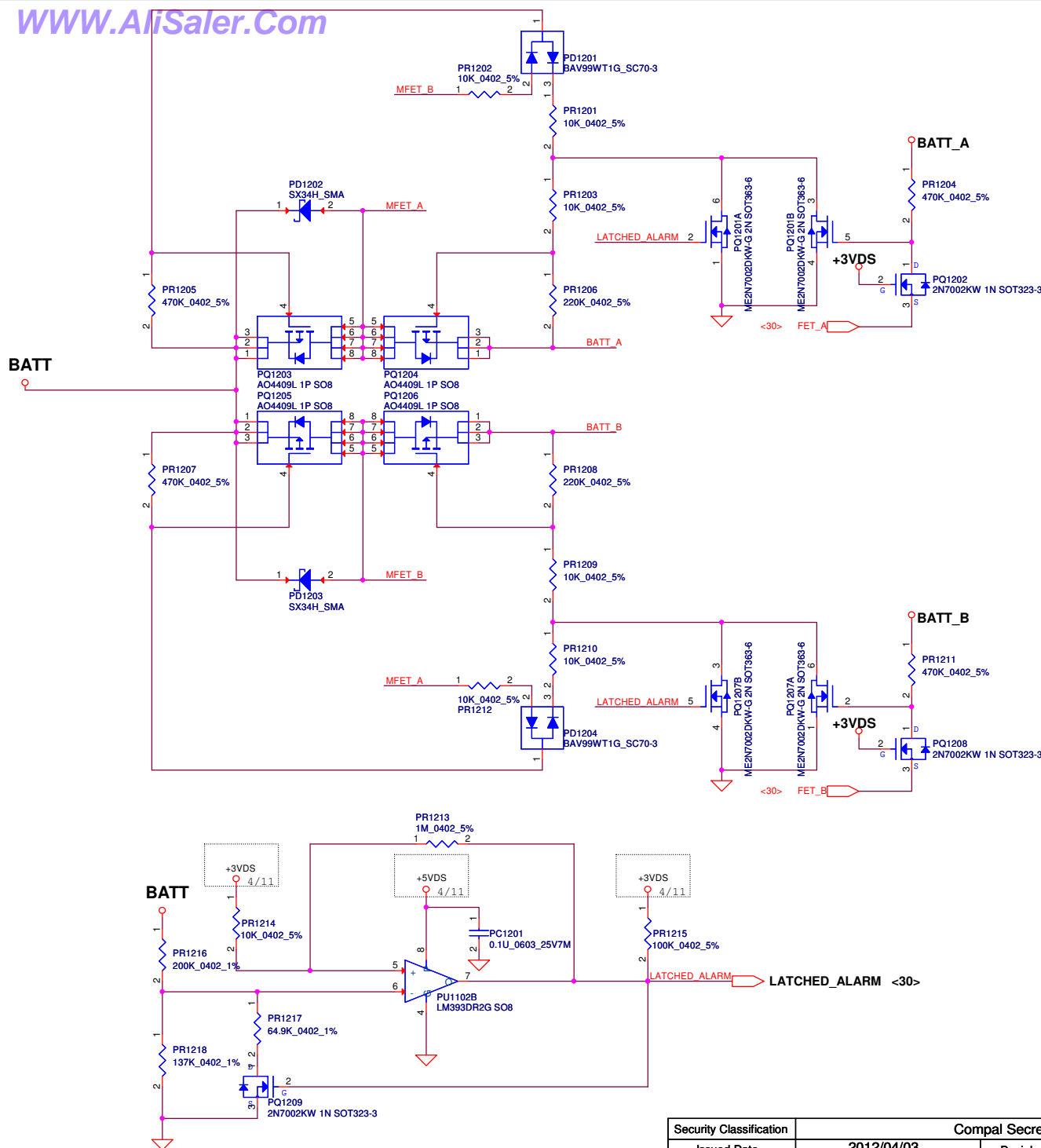
+1.5VS

+1.5V_PCIEP
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Peak Current=0.66A

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Version Change List (P. I. R. List) for HW Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	30	KBC	08/18	HP	The quad-mode does not require any GPIO from KBC	Delete R1348 & R1349 and Add R541 and R542	0.2
2	31	PWR_OK	08/18	HP	Makes the power good circuit working.	Non-install R284	0.2
3	26	MXM	08/28	Compal	MXM Card can't be recognized in OS.	Change U37 to MC74VHC1G08DFT2G (Non-OD type)	0.2
4	36	Switch/MUX	09/07	HP	Move D-Sub connector on M/B	Add VGA filter circuit and connector	0.2
5	30	KBC	09/08	HP	SUSCLK is off during DS3 condition	Add Y4, C423, C424 ; Delete R258, R264	0.2
6	30	KBC	09/08	HP	Simplify the KBC solution for MEC1322	Delete R262, R266, R219, R216, R241, R242, R271, R253	0.2
7	25	NGFF	09/08	HP		Add PU resistor for WWAN_FULL_PWR/WWAN_RSVD2	0.2
8	39	NFC	09/10	HP	KBC detection of NFC module	Add 200K (R1377) PD resistor to NFC_VARI_RX	0.2
9	39	NFC	09/10	HP	Power rail option for NFC module	Add +3VM_LAN (R1376) for NFC module	0.2
10	9	CPU	09/11	HP		Remove RC102 and RC103	0.2
11	20	PCH	09/11	HP	Connect PCH's pin AD12 to +3V_PCH directly	Remove RH226	0.2
12	5	CPU	09/11	HP	Connect CPU_AT26 pin to CPU_PLTRST# directly	Remove RC66	0.2
13	5	CPU	09/11	HP	Connect CPU_AL34 pin to H_CPU_PWRGD directly	Remove RC30	0.2
14	9	CPU	09/11	HP	Connect SLP_S3# to QC5.5 directly.	Remove RC93	0.2
15	33	DOCKING	09/11	HP	Connect EN_P1V5 to JDOCK1.140 directly.	Remove R351	0.2
16	33	DOCKING	09/11	HP	Connect ON/OFFBTN_KBC# to Docking directly.	Remove R336	0.2
17	15	PCH	09/11	HP	Simplify PCH solution for PCIE CLK Group	Remove RH107, RH103, RH114, RH116, RH122 RH124, RH126, RH127, RH129, RH130	0.2
18	14	PCH	09/11	HP	Reassignment GPIO for "BT_OFF"	Change it from GPIO72 to GPIO61	0.2
19	30	KBC	09/11	HP	Reserve for SUSACK# signal	Uninstall R436 and add R1378	0.2
20	18	PCH	09/11	HP	Reassigned BRD_ID4 to GPIO40 for CP support and update table for DB1-R	Connect RH180.1 to +3VS & RPH1.8 to GND	0.2
21	30	KBC	09/12	HP	Simplify the KBC solution for MEC1322	Delete R249, R251, R256, R277	0.2
22	36	Switch/MUX	09/12	HP	eDP trace length over Intel's specification	Change solution to PS8321	0.2

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